Fabrication of SOI MEMS Inertial Sensors with Dry Releasing Process

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Abstract—In this paper, a dry releasing process for making high aspect ratio SOI MEMS devices is presented. The proposed process can not only avoid the stiction effects which will cause the device failure, but also partially suppress the footing effect during the deep reactive ion etching (DRIE) of the device structures. The basic idea is to use the pre-defined releasing hole to completely remove the buried oxide underneath the device just before the final structure etching, therefore avoid the wet process during the structure release. The on-chip testing structures for etching end point of DRIE are also designed to precisely monitor the etching results. A capacitive accelerometer was fabricated and tested using the proposed process. The preliminary results imply the dry releasing process can effectively avoid the stiction problem.

INTRODUCTION

With the development of DRIE (Deep Reactive Ion Etching) technology, the bulk micromachining capabilities of silicon MEMS technology make great process. The silicon-on-insulator (SOI) wafers also show many advantages over conventional silicon substrate for both microelectronic devices and micro-electromechanical devices. SOI wafers in combination with DRIE technology can realize high aspect ratio single crystal silicon structures with uniform thickness and low build-in stress, which are attractive for making high performance MEMS inertial sensors that prefer large proof mass and sensing capacitances. Various SOI MEMS processes have been developed [1-6]. The most straightforward method is to define the structure by DRIE from the structure layer of SOI wafer, followed by sacrificial wet etching of the buried oxide layer with HF solutions [1]. However, the stiction problem during the wet etching will affect the process yield, and requires special process and equipments to solve it.

Dry releasing processes are particularly desirable to avoid the stiction problems encountered in wet releasing process. The vapor HF etching can be used to release the MEMS devices without stiction [2], but special equipments are required for good control and safety. Layout controlled dry etching and release techniques with single mask were developed to free the MEMS structure by application of the notching effect of DRIE [3,4], but the thickness uniformity of MEMS devices may be affected. The backside cavity etched by DRIE or anisotropic wet etching can also be used to release the structures without wet etching [5,6], but etching through the wafer with DRIE is time-consuming and expensive, and anisotropic wet etching will need more device areas due to the inclined sidewall.

In this paper, a dry releasing process for making high aspect ratio SOI MEMS devices is presented. The proposed process can not only avoid the stiction effects which will cause the device failure, but also partially suppress the footing effect during the DRIE of the device structures. The on-chip testing structures for etching end point of DRIE are also designed to precisely monitor the etching results. A capacitive accelerometer was fabricated and tested using the proposed process. The preliminary results imply the dry releasing process can effectively avoid the stiction problem.

PROCESS DESIGN

The process and partial layout of the SOI MEMS devices for two-mask releasing process are shown in Fig.1 and Fig.2. The aluminum (Al) mask and photoresist (PR) mask are used to define the device structures and releasing holes respectively. At first, a 1.6 µm Al layer is sputtered and patterned to define the final device structures (Fig.1a). The Al layer is also used as interconnections and electrical pads. Then, photoresist is spun and patterned to define the releasing holes (Fig.1b), as that shown in Fig.2, which are at least 2 µm smaller than the device structure holes at each side. Next, the first DRIE is carried out to etch the releasing holes partially (Fig.1c). The trench depth etched depends on the total structure thickness, device patterns, etc. Then, the photoresist is removed, and the second DRIE is performed to release the structures completely (Fig.1f). Because no further wet processes are needed, the stiction problem can be completely avoided.
The proposed process can also suppress the footing effect after the final releasing DRIE, which is depicted in Fig.3. After the second DRIE, the releasing holes are etched to the buried oxide layer. If the DRIE have no anti-footing add-ons, the footing problems will occur at the corner of the trenches (Fig.3a). If the etching conditions are well controlled, the lateral undercut caused by footing problems will be not too much. After the final releasing DRIE, the structures with undercut will also be completely removed (Fig.3b), so the structures with vertical sidewall (no undercut) will be realized.

Figure 2. Schematic layout of the device structures.

Figure 3. Schematic of the anti-footing method. (a), after the second DRIE. (b), after the final releasing DRIE.

EXPERIMENTS

In our experiments, (100) oriented 4 in. SOI wafers with 40 μm structure layer, 2 μm buried oxide and 400 μm handle layer are used. The all DRIE steps are carried out by STS ASE™.

In order to precisely monitor the etching stop point, which is very important for the proposed process to ensure that the releasing holes are etched through without too much over-etching, on-chip testing structures are designed and used in our experiments. One testing structure is based on the footing effect, as that shown in Fig.4a. Microbeams with different widths and similar spaces with releasing holes are designed to monitor the etching depth. Once the trenches are etched through, further etching will undercut the microbeams due to the footing effect, and finally release the microbeams under too much over-etching. By carefully choose the sizes of the microbeams and spaces, when the releasing holes are etched through, only the microbeams with widths less than specific dimensions are released. Therefore, such structures can be used to determine the etching through point. Another testing structure is based on the resistance measurement, as that depicted in Fig. 4b. If the trench between two adjacent structures was etched through, the measured resistance will become infinity. As long as the structure dimensions and spaces are properly chosen according to the releasing holes,
the on-chip testing structures can be used to monitor the etching end point.

Figure 4. Etch stop detection structure. (a), using footing effect, (b), using resistance measurement.

Another important issue is the wet etching of the buried oxide layer. Because the Al layer is used as mask and electrodes in our experiment, the etchant must have high selectivity between oxide and Al. In order to increase the etching selectivity, a mixture of buffered hydrofluoric acid (BHF) and glycerol is used with optimized etching conditions [7]. The etchant solution consists of 1 volume of 40 wt.% hydrofluoric acid (28ml), 4 volumes of 40 wt.% ammonium fluoride (112ml) and 2 volumes of glycerol (56ml). The mixture was then agitated by a temperature controllable water-bath with magnetic stirring bar. From the experimental results shown in Fig.5, the etching selectivity is increased with elevated temperature. Considering the stability, the releasing etching was performed at about 60 °C.

Because the releasing holes are 40 µm or more deep, the bubbles generated by the etching process can not be completely released from the trench bottoms even with the agitation of magnetic stirring bar, therefore affect the etching rate and uniformity. In our experiment, a temperature controllable ultrasonic bath was used instead, which can efficiently remove the bubbles.

Figure 5. Al and SiO$_2$ etching rate as a function of temperature.

RESULTS AND DISCUSSIONS

Figure 6. Cross section view of the SOI structures fabricated by two-mask dry release process. (a), before the oxide etching, (b) after oxide etching.
The cross sectional views of the SOI device structures after second DRIE and after oxide etching are shown in Fig.6. The backside of the released microstructures is shown in Fig.7. The results show that the footing problem can be suppressed effectively, especially at the narrow gap of the comb fingers.

![Image](image1)

Figure 7. Backside of the released microstructures.

In order to verify the dry releasing process, a capacitive accelerometer with 40 µm device layer was designed and fabricated. The fabricated accelerometer is shown in Fig.8. The capacitance change according to the voltage applied between the movable and fixed electrodes was measured and shown in Fig.9. The preliminary results indicate that the accelerometer has been completely released, and the dry releasing process can be used to fabricate various MEMS devices.

![Image](image2)

Figure 8. SEM photo of the fabricated accelerometer.

One possible drawback of the proposed process is that the substrate is not flat because it is etched during the final releasing DRIE, as that shown in Fig.1f and Fig.6b. The non-flat substrate may influence the capacitance change of capacitive inertial sensors. In order to overcome this problem, another Al layer can be sputtered at the backside of the SOI wafer as electrodes and connected with the movable structures to minimize the effect of parasitic capacitors.

![Image](image3)

Figure 9. Sensing capacitance vs. driving voltage of the accelerometer.

CONCLUSION

A two-mask dry releasing process for making high aspect ratio SOI MEMS devices is presented. A capacitive accelerometer was fabricated and tested using the proposed process. The preliminary results indicate the dry releasing process can not only effectively avoid the stiction problem, but also partially suppress the footing effect during the DRIE of the device structures.

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REFERENCES


