ELSEVIER

Sensors and Actuators B 78 (2001) 180–190

SENSORS AND ACTUATORS B CHEMICAL

www.elsevier.com/locate/sensorb

Design and simulations of SOI CMOS micro-hotplate gas sensors

F. Udrea[a,*], J.W. Gardner[b], D. Setiadi[a], J.A. Covington[b], T. Dogaru[a], C.C. Lu[a], W.I. Milne[a]

[a]*Engineering Department, Cambridge University, Trumpington Street, Cambridge CB2 1PZ, UK*

[b]*Division of Electrical and Electronic Engineering, School of Engineering, University of Warwick, Coventry CV4 7AL, UK*

Abstract

This paper describes a new generation of integrated solid-state gas-sensors embedded in SOI micro-hotplates. The micro-hotplates lie on a SOI membrane and consist of MOSFET heaters that elevate the operating temperature, through self-heating, of a gas sensitive material. These sensors are fully compatible with SOI CMOS or BiCMOS technologies, offer ultra-low power consumption (under 100 mW), high sensitivity, low noise, low unit cost, reproducibility and reliability through the use of on-chip integration. In addition, the new integrated sensors offer a nearly uniform temperature distribution over the active area at its operating temperatures at up to about 300–350°C. This makes SOI-based gas-sensing devices particularly attractive for use in handheld battery-operated gas monitors.

This paper reports on the design of a chemo-resistive gas sensor and proposes for the first time an intelligent SOI membrane microcalorimeter using active micro-FET heaters and temperature sensors. A comprehensive set of numerical and analogue simulations is also presented including complex 2D and 3D electro-thermal numerical analyses. © 2001 Elsevier Science B.V. All rights reserved.

Keywords: Design; Simulations; SOI CMOS

1. Introduction

Of late there has been an increasing demand for portable, handheld gas monitors, mainly for application within the environmental, automotive and medical industries. Present portable instruments are limited because electrochemical cells cannot detect low levels of hazardous gases, while solid-state resistive materials (e.g. stannic oxide) are more sensitive but require operation at high temperatures. This results in a power consumption of ca. 1 W and makes these resistive sensors unattractive for application in battery operated and automotive units.

The most common type of commercial high temperature solid-state gas sensor is based upon a resistive element (e.g. the Taguchi gas sensor). This measures the change in electrical conductance of a porous, sintered metal oxide film on exposure to the target gas. The layout of this sensor basically comprises a heater and a pair of electrodes covered by a metal oxide film. In order to achieve fast response times, the sensors are operated at high temperatures (300–500°C), although this consumes considerable power [1].

Attempts to combine these high temperature materials with a standard silicon process have only been partially successful. Silicon resistive sensors operating at these temperatures usually suffer from poor thermal stability and durability. Gardner et al. have designed sensors using composite structures with a platinum resistive heater embedded in low stress silicon nitride with electrodes exposed for metal oxide deposition [2]. Other sensors have been reported based on nitride or oxynitride, membranes including microcalorimeters [3–7]. Although these sensors have shown excellent thermal stability as well as the durability to withstand thermal cycling, the process is not fully CMOS compatible, and so suffers from a higher cost to fabricate and does not offer the possibility of circuit integration. Resistive heaters based on a polysilicon resistor have been reported, although these devices tend to suffer from two major short falls. Specifically the high doping levels required for the polysilicon resistor puts significant stress into the membrane, and they show poor long term thermal stability. CMOS compatible sensors have been successfully fabricated by Suehle et al. [8] through a commercial foundry (MOSIS). These sensors are based on oxide Al micro-hotplates and polysilicon heaters. Al tends to limit the temperature operation due to electro-migration and the existence of an Al hotplate leads to increased power losses. The temperature is evaluated in a standard way, by measuring the change of the resistance of the polysilicon. Recent work carried out by Gajda et al. [9] and Gajda and Ahmed [10], using SIMOX

* Corresponding author.
E-mail address: fu@eng.cam.ac.uk (F. Udrea).

0925-4005/01/$ – see front matter © 2001 Elsevier Science B.V. All rights reserved.
PII: S0925-4005(01)00810-3

(SOI) micro-hotplates, shows the potential applications of this technology for pressure sensors, chemical and flow sensors. In [9] the use of a MOSFET test structure and a standard silicon heater on a silicon/oxide membrane is also demonstrated. These results are very interesting and show the variation of threshold voltage with the temperature and the stress induced in the membrane. The MOSFET however is not explicitly used as a Gas-FET and certainly not used as a heater. The experimental demonstration is based on a simplified CMOS-type process with five photolithography steps and neither standard CMOS devices nor circuits are shown. Very recently, Briand et al. [11] have demonstrated a Gas-FET sensor on a nitride membrane with a silicon island placed underneath operating at 200°C. These results are very encouraging and show the potential of micromachined membrane FETs in gas sensing applications. All of these previous proposals are based on purely resistive heaters that employ current control. They do not feature integrated CMOS devices and circuits although, in some cases, a CMOS compatible process is used. While SOI technology has been previously investigated for making micro-hotplates based on front side etching with a simplified CMOS process [9], there are no reports on the use of SOI in a standard CMOS foundry such as Europractice, which features a complex fabrication process. In addition there are no studies of CMOS SOI-based membranes using back-side micromachining, and no design of chemo-resistive or microcalorimeter gas-sensors is present. Furthermore, there is a general lack in literature of 2D & 3D numerical simulations of electro-thermo-mechanical analyses of micro-hotplates.

Gardner and co-workers have suggested the use of MOSFET heaters based on silicon-on-insulator (SOI) technology [12,13]. This is of significant importance since, unlike in previous studies, the temperature can be controlled accurately via a MOSFET gate.

By proposing the design of a micro-hotplate using SOI technology, both the CMOS heater and gas sensitive material can operate at much higher temperatures (up to 350°C) than would normally be expected for a CMOS process. MOSFET gas sensors based on a standard silicon process can only operate up to about 200°C (typically 175°C), above which the junctions break down and so give poor device stability. Also, by using SOI technology, the process is completely CMOS compatible permitting the integration of sophisticated control and signal conditioning circuitry with the sensing element. This will also reduce the cost of fabrication, producing high quality and repeatable heater structures. Furthermore, this circuitry would benefit from the well-known advantages of low power SOI technology, namely, simple and efficient isolation, reduced leakage currents, reduced parasitic capacitances and reduced short channel effects [14]. Besides, SOI is ideal for use in smart CMOS-compatible sensors since the buried layer acts as an effective etch-stop to define the membrane. Finally, the buried oxide combined with LOCOS or multiple trench isolation in the membrane area offers excellent thermal insulation reducing the thermal conduction losses to negligible levels. The only remaining losses are convective and radiative losses to air, the latter term being negligible below 400°C.

This paper presents the design and numerical simulations of the high temperature MOSFET micro-hotplate gas sensors based on SOI technology, including 2D and 3D electro-thermo-mechanical simulations, using the ISE-TCAD^{TM} [15] package and the SPECTRE-S module from Cadence. The fabrication process and preliminary experimental results are also briefly discussed.

2. SOI micro-hotplate sensor structures

The basic structure of the device can be described as a MOSFET micro-hotplate heater lying within a SOI membrane. The oxide layer, as a standard part of an SOI structure, serves three purposes: it acts as an etch stop for the etching process, thermally isolates the sensing area reducing the high power losses associated with silicon, and provides a high level of electrical isolation for any associated electronic circuitry. Associated electronic circuitry would be placed outside this membrane area so as to reduce any effects brought about by the high temperatures involved.

We propose here two major types of smart sensors. The two types have similar features but are essentially different in operation. Both structures feature a micro-heater in the form of a self-heating FET. The FET heater is essentially either an n-channel or p-channel MOSFET in CMOS technology and therefore does not require any extra fabrication steps to the standard CMOS process.

1. The first structure (Fig. 1) is a *SOI chemo-resistive gas sensor* which consists of a sensing element (a thick porous film (2–10 μm) Pd doped SnO_2) deposited onto two metal electrodes (metal 2 layer), which are preferably made of gold and separated from the heater through a passivation layer (the gold layer is put down and patterned after the CMOS sequence is completed). The operation of this sensor is based on the change in

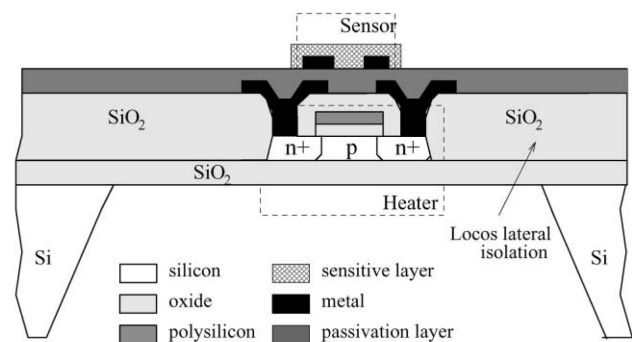

Fig. 1. Structure of a resistive gas sensor with an *n*-channel MOSFET heater based on thick CMOS SOI technology (not to scale).

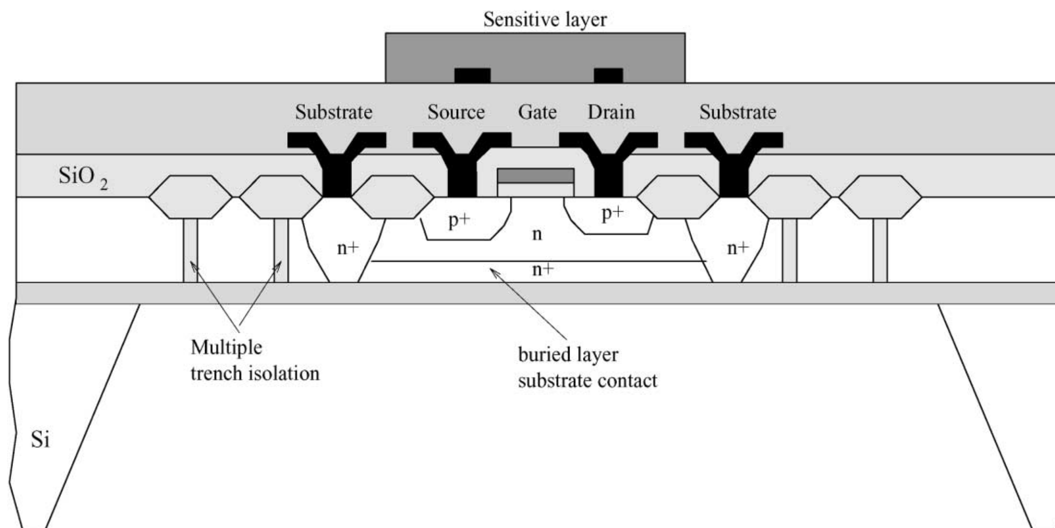

Fig. 2. Structure of a resistive gas sensor with an *p*-channel MOSFET heater based on thick CMOS SOI technology (not to scale).

resistance of the sensing element at high temperatures, when exposed to a gas. There are two technologies available, function of the thickness of the SOI layer. The first is the thin SOI technology with the thickness of the top silicon layer <0.4 μm. This technology uses LOCOS layers for lateral thermal and electrical isolation as shown in Fig. 1. Fully depleted (FD) MOSFETs built in this technology are known to have excellent electrical and thermal properties such as increased inversion layer charge, reduced parasitic bipolar effect, improved subthreshold regime and high temperature operation. Integrated circuits built in this technology (e.g. operational amplifiers) have been demonstrated to operate at extremely high temperatures: 400°C [14] well above the limit of 175°C characteristic of bulk CMOS. The second is the thick SOI technology where the silicon layer thickness is >0.5 μm. The MOSFETs built in this technology are either partially depleted (PD) or non-depleted depending if the depletion region associated with the gate transversal electric field is reaching or not the buried oxide layer. This technology uses trenches filled with oxide for isolation. Since the width of the trench is limited by the technological process, several such trench rings have to be used within the membrane surrounding the sensing area of the device to prevent lateral thermal conduction to the circuit area. Fig. 2 shows an SOI smart sensor based in BiCMOS thick SOI technology. A *p*-channel MOSFET micro-heater is used with the substrate contacted via an $n+$ buried layer to suppress the action of the parasitic PNP transistor acting in parallel with the MOSFET and thus increase the temperature range.

2. The second type of smart sensors proposed here is the *SOI microcalorimeter sensor.* A schematic diagram and a cross-section of it and the integrated basic CMOS cells placed outside the membrane are shown in Figs. 3 and 4, respectively. As stated above, the microcalorimeter can also use a thicker SOI layer with concentric oxide trench rings to minimise the power losses and prevent thermal interference between the sensing area and the electronic area. A forward biased *p–n* diode acts as a temperature sensor and is placed at the centre of the MOSFET heater. At high temperatures, the gas reacts with gas (e.g. methane) on the surface of the catalyst. The chemical power generated results in a temperature rise in the sensing area which is picked up by the thermo-diode and converted into a voltage difference. It is possible to remove common thermal and electrical effects by using a second identical membrane structure with the same thermal mass as a reference (the catalyst is inactive) and operate the two structures in a differential mode as shown in Fig. 5. The differential amplifier is placed outside the membrane and can measure with high precision the difference in the voltage drops of the two thermo-diodes. The output voltage is proportional with the differential temperature rise and therefore with the

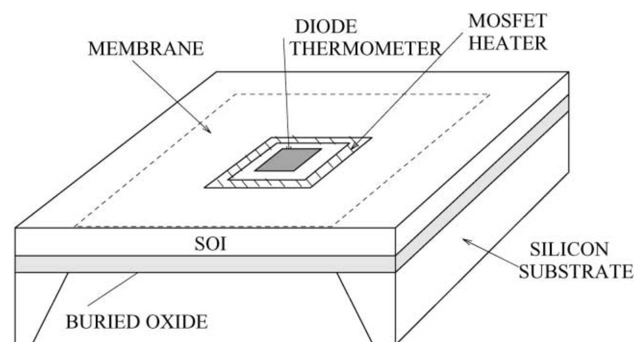

Fig. 3. A schematic diagram of a microcalorimeter placed on a thin SOI membrane showing the MOSFET heater surrounding the thermo-diode (catalyst not shown).

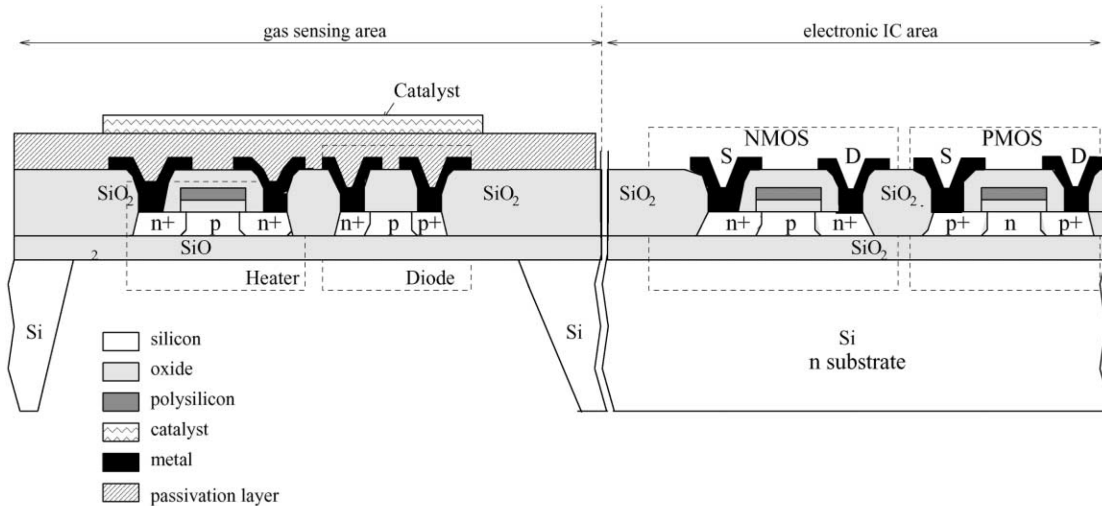

Fig. 4. The cross-section of a CMOS SOI microcalorimter showing a CMOS MOSFET heater and a diode together with adjacent CMOS cells placed outside the membrane. The MOSFET heater is done at the same time with the 'electronic' MOSFETs in CMOS technology (not to scale).

gas concentration. The use of SOI CMOS MOSFETs and diodes as heaters and temperature sensing elements, respectively, yields excellent thermal and electrical matching properties between the active cells and the reference without the need for manual "sorting".

Extensive 2D & 3D electro-thermal numerical simulations using ISE-Solidis & Inspec [15] have been carried out to assess the over-all performance of these sensors.

3. 2D electro-thermal device simulation

The ISE — Inspec simulator accounts for the fully coupled current–lattice temperature equations and the degradation of the MOSFET channel mobility with the temperature. For simplicity we have simulated in 2D one single MOSFET finger placed on a SOI membrane to show the self-heating effect and relate the temperature rise to the power dissipated by the MOSFET. Fig. 6 shows the lattice temperature and power consumption as a function of gate voltage V_{GS} for a fixed V_{DS} of 5 V. The operating temperature within the sensing area is set accurately by the voltage applied to the MOSFET gate. The lattice temperature of the micro-hotplate is shown to increase almost linearly with the applied gate voltage — provided that the gate voltage is above the threshold voltage (typically 0.7 V). Hence, the power consumption of the heating element is also approximately linear with lattice temperature and is less than 2.5 mW at a lattice temperature of 400°C. It must be remembered that this simulation shows the temperature of the lattice for one single MOSFET finger in 2D. A typical membrane will contain at least five such fingers. Moreover,

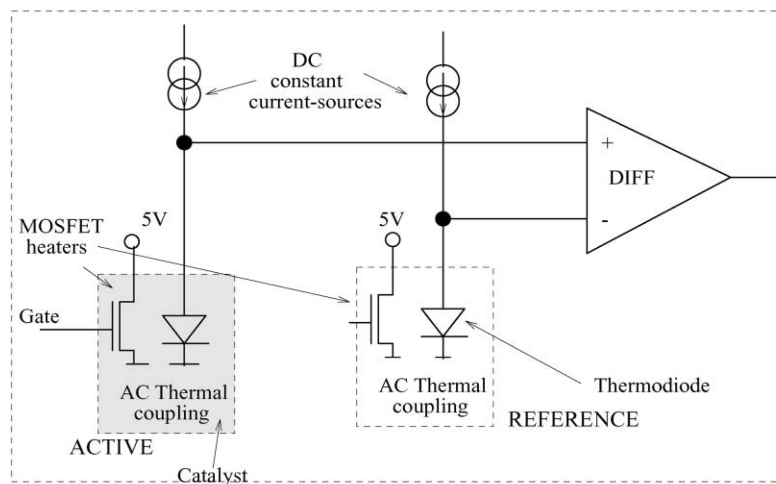

Fig. 5. A simple differential transducing circuit for the smart SOI microcalorimeter (showing NMOS version only). Current sources are identical when obtained from a current mirror circuit.

the results are obtained using a 2D simulation, while a different result (a lower lattice temperature for the same power consumption) will be expected when the device is simulated in 3D. From these numerical simulations, it is clear that varying the gate voltage can be simply used to control the lattice temperature, where the lattice temperature changes almost linearly with the power consumption. The operating temperature in the sensing area for a given input power, however, depends on the heater area, the final membrane thickness, the thermal properties of the materials present in the membrane, the efficiency of the lateral thermal isolation within the membrane and, to a less extent, the layout of the MOSFET heater.

4. 3D electro-thermal device simulations

An electro-thermal simulation calculates the heat loss through the membrane and to the air from the self-heating effects brought about by electrical current flowing through the MOSFET. A Joule heating term enhances the heat transfer equation, while the electro-resistive equation exhibits a temperature-dependent electrical conductivity, as described in the following equations:

$$\nabla \cdot (\kappa(T)\nabla T) + \frac{J^2}{\sigma(T)} = 0 \quad (1)$$

$$\nabla \cdot (\sigma(T)\nabla \Psi) = 0 \quad (2)$$

where σ is electrical conductivity, Ψ the electroresistive potential, κ the thermal conductivity, T the temperature, and $J = \sigma\nabla\Psi$ denotes the electrical current density. The temperature along the bottom of the silicon wafer is equivalent to an ideal heat reservoir of the ambient temperature (Dirichlet boundary condition):

$$T = 300\,\mathrm{K} \quad (3)$$

The temperature gradient in the air at the membrane/air interface can be approximated by Newton's law of cooling:

$$\kappa(T)\nabla T = -h(T - T_0) \quad (4)$$

where h denotes a surface heat transfer coefficient and T_0 is the constant ambient temperature. For the upper surface of the membrane, the surface heat transfer coefficient h has been set to a value of $125\,\mathrm{W/m^2\,K}$, while for the lower surface, $h = 60\,\mathrm{W/m^2\,K}$ [14]. If the temperature variation on the surface of the self-heating MOSFET is not very pronounced, an averaged heat transfer coefficient corresponding to the average surface temperature can be introduced. The typical parameters for the SOI membrane structure are given in Table 1 and the physical constants used in the simulations are shown in Table 2. It has been shown experimentally by Astie et al. [16] that the thickness of the silicon membrane must be kept above 3 μm in order to reach acceptable values of fabrication yield (>90%) and prevent serious mechanical breakdown under operation. The total thickness of the membrane proposed here is ca. 7 μm, and so both a high yield and good robustness can be expected.

Table 1
Geometrical and process parameters used in the SOI gas sensor simulations

Description	Value
Tin oxide thickness	10 μm
Epi-layer thickness	1200 nm
Buried oxide (SOI substrate) thickness	400 nm
Gate oxide thickness	17.5 nm
Oxide thickness between metals and polysilicon	700 nm
Oxide thickness between metal 1 and metal 2	1200 nm
Polysilicon thickness	500 nm
Metal 1 thickness	740 nm
Metal 2 thickness	1050 nm
Passivation thickness	1800 nm
Substrate thickness	475 μm
Membrane area	500 μm × 500 μm
Heater area	300 μm × 300 μm
Sensing area (tin-oxide)	100 μm × 100 μm

The mechanical stability (i.e. low residual stress) of the silicon/oxide membrane is crucial for viable sensors. Oxide and nitride based membranes have been reported to provide good mechanical stability and offer high yield [3–11]. However, the thermal and pressure-related stress as well as the residual stress have also to be considered. Although in theory the oxide has a compressive stress its intrinsic value is significantly dependent on the initial SOI wafers and the process used. Deposition of a thin layer of nitride, which has a tensile stress [3,9], can compensate for this stress, nevertheless this solution needs further investigation. A numerical study of the thermal and pressure type stress in the SOI membrane and the maximum deflection of the membrane at high temperatures as a function of the aspect ratio of the membrane has been reported by us elsewhere [17]. However, this study did not consider the contribution of the residual stress which, as already mentioned, is highly dependent on the fabrication process.

There are three heat transfer mechanisms, conduction, radiation and natural convection. Measurement results by

Table 2
Physical properties of the materials used in the SOI gas sensor simulations [15–17]

Material	Thermal conductivity (W/m K)	Specific heat (J/kg K)	Density (kg/m^3)
Tin oxide	35	896	7267
Silicon	157	700	2330
Buried oxide (SOI substrate)	1.2	730	2270
Silicon oxide	1.2	730	2270
Polysilicon	28	750	2330
Nitride	19	750	3440
Aluminium	236	904	2699
Air	0.024	1030	1.1

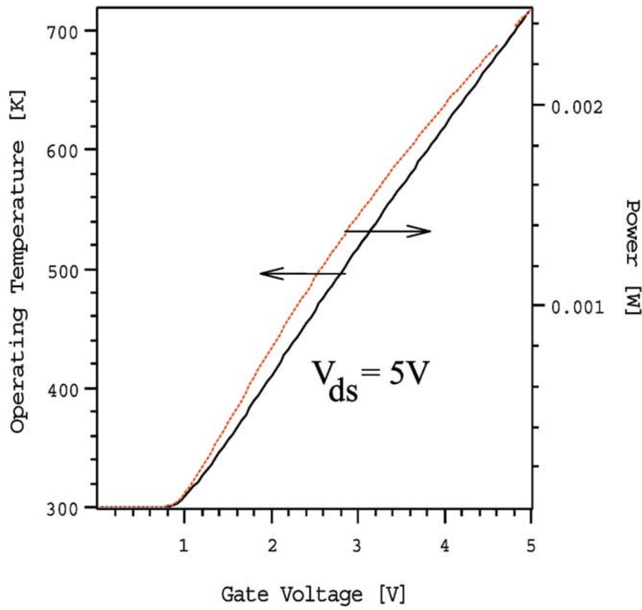

Fig. 6. Lattice temperature and power consumption of *n*-type SOI MOSFET heater as a function of the gate voltage.

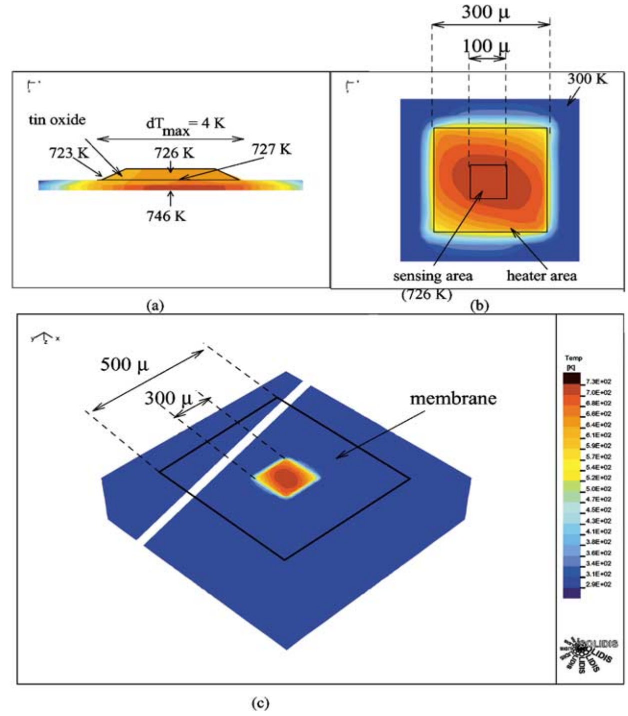

Fig. 7. 2D temperature distribution in the SOI membrane (ISE-Solidis simulations). The asymmetric profile is associated with significant heat loss via the asymmetric metal layers near the surface. The influence of the metal layers is less in other structures.

Gotz et al. have shown that for a very thin membrane and side length smaller than 5 mm, radiation can be neglected and the heat transfer to the gas is dominated by conduction, while fluid motion does not contribute significantly [18]. Pike and Gardner have also presented a similar result for hotplates operating below 350°C [19]. The radiation losses therefore have been considered as negligible for our simulations. Although the heat conductivity of the air is small compared to the silicon, the air is the most important path for the power losses because of the large area in contact compared to the membrane cross-sectional area bordering the sensor. Pike and Gardner [19] have also shown that the

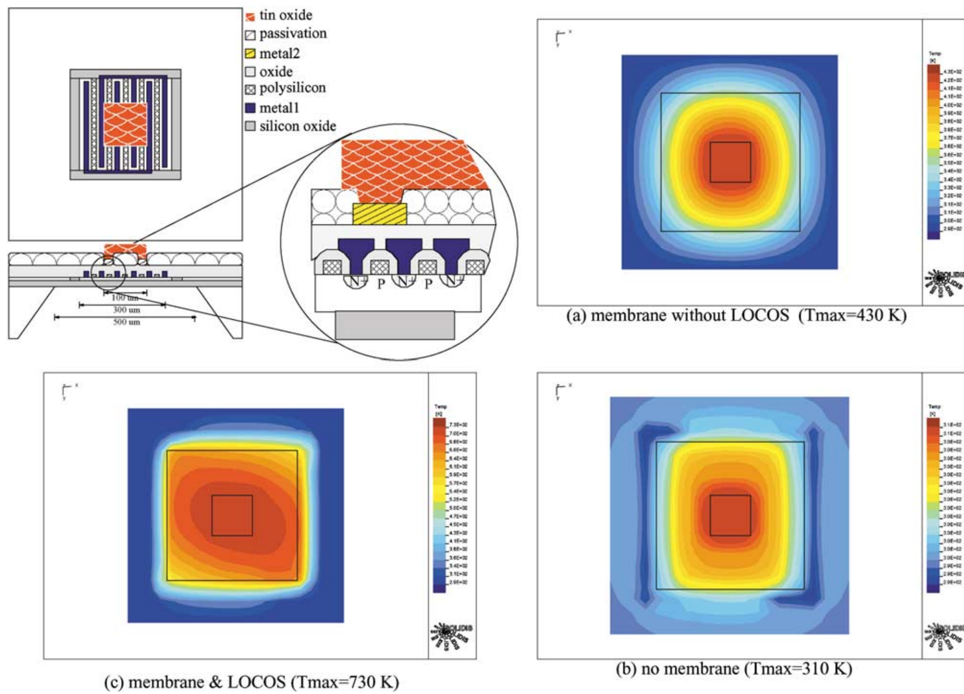

Fig. 8. Temperature profile of a resistive gas sensing using an interdigitated MOSFET heater for an SOI membrane without LOCOS (a); an SOI substrate — no membrane (b); and an SOI membrane & LOCOS isolation (c) for the same input power.

convective heat loss is a significant proportion (about 2/3) of the total heat loss of the micro-hotplate above a temperature of about 50°C above ambient.

The simulations have been carried out assuming the following boundary conditions: (a) the temperature along the bottom side of the silicon wafer is equivalent to the ambient temperature, (b) on the upper and lower surfaces of the membrane, heat is dissipated through convective exchange with air, and (c) radiation losses have been considered as negligible. The simulator accounts for the temperature dependence of the silicon's thermal conductivity, by using:

$$\kappa(T) = \kappa_0|_{T_0} + \left.\frac{\partial\kappa}{\partial T}\right|_{T_0}(T - T_0) \quad (5)$$

The temperature contour within the membrane is shown in Fig. 7 for an input power of 35 mW. It is worth pointing out that a temperature gradient is only observed within the membrane while the temperature of the bulk silicon remains constant and equal to the ambient temperature. The LOCOS layer surrounding the membrane prevents significant heat conduction throughout the membrane. Therefore, any signal condition circuitry placed outside the membrane would operate at an ambient temperature. A similar effect may be achieved using multiple oxide trenches for the thick SOI membrane, although it is expected that a slight increase in the heat losses will occur because of the lower thermal resistivity of the multiple trench layers compared to the full LOCOS isolation. Fig. 7 also shows that a maximum temperature gradient of 23 K is observed between the core of the heater (MOSFET device) and the sensing element. Within the sensing element a 4 K variation in temperature is found, with a temperature of 723 K at the borders, 726 K at the top and 727 K at the bottom.

To assess the effectiveness of the membrane and the LOCOS isolation, 3D thermal simulations have been performed for two other structures. First using an SOI membrane without LOCOS (a) and second using a typical SOI substrate without a membrane (b). These can be compared to our design (c) for the same input power as shown in Fig. 8. From this figure it is evident that the combination of the SOI membrane and LOCOS isolation is very effective in reducing the heat conduction losses and therefore achieving high temperatures in the sensing area with low power consumption.

The power consumption is also dependent on the heater area as can be seen in Fig. 9. In order to minimise the power consumption the heater area should be reduced, however, this leads to a reduced sensing area and therefore lower sensitivity.

5. Analogue device and circuit simulations

We have performed extensive device and circuit simulations using the Spectre-S simulator available in Cadence. These simulations have been carried out through direct extraction of the active and passive components (including parasitic elements) from the final layout design and therefore their accuracy is very high.

We have simulated first the behaviour of the FET heater and the response of the thermo-diode with temperature. Thus, we assessed the maximum temperature the MOSFET can reach before the parasitic parallel transistor is activated.

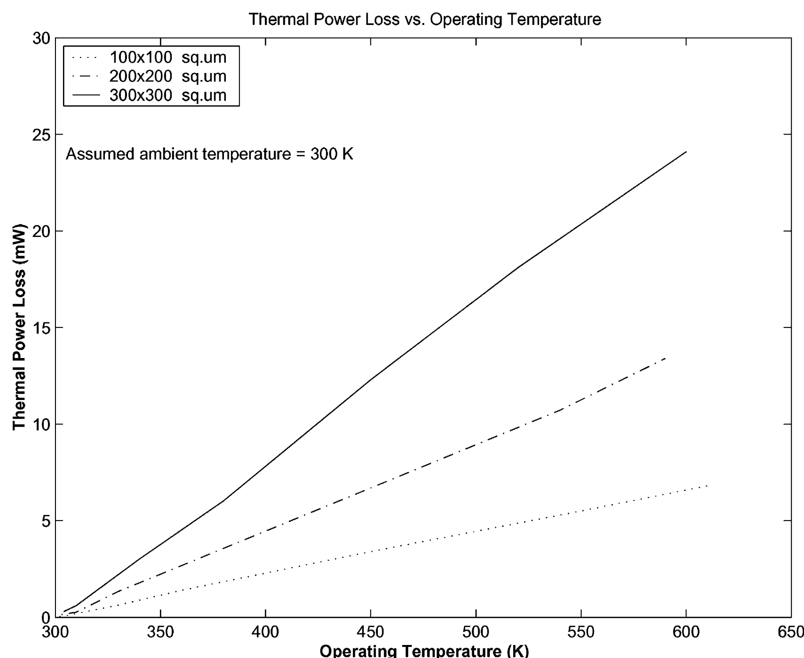

Fig. 9. Power consumption vs. operating temperature for three different heater areas.

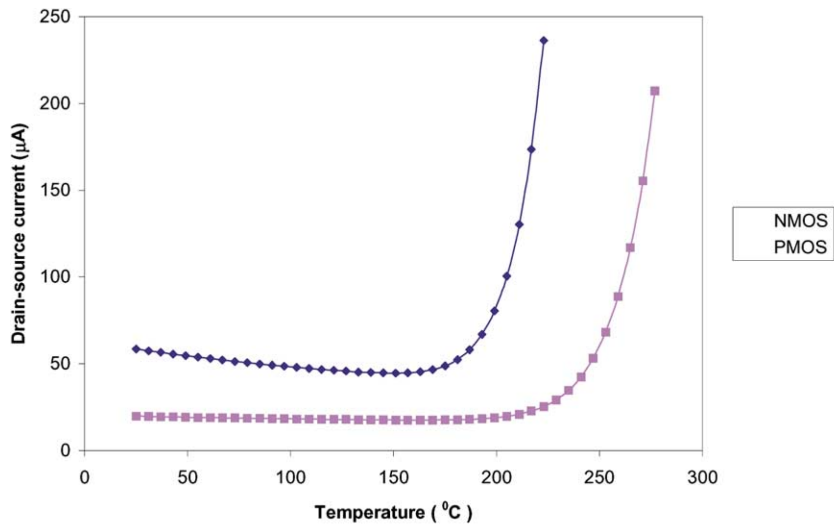

Fig. 10. Drain-source (source-drain) current as a function of temperature for a fixed drain and gate voltage for *n*-channel (and *p*-channel) MOSFETs in thick BiCMOS SOI technology.

Interestingly, we found that in the thick SOI Bi-CMOS technology, the *p*-channel MOSFET heater has superior thermal characteristics over the n-channel MOSFET. The *p*-channel MOSFET has an improved substrate contact, via an $n+$ buried layer (Fig. 2), and hence can operate at higher temperatures than an *n*-channel MOSFET. This is because the body diode is inhibited by the presence of a good Ohmic substrate contact to the highest potential in the circuit.

Fig. 10 compares the analogue simulations of the *n*- and *p*-channel MOSFETs operated in DC in similar conditions at a variable temperature (up to 300°C). The PMOSFET heater reaches 250°C while the control on the gate is still maintained. Control is possible at higher temperatures is possible using the drain voltage. The maximum temperature given by Spectre-S is for a simple *p*-channel MOSFET in thick (1.2 μm) SOI technology. We therefore expect that a *p*-channel MOSFET heater lying on a membrane (with the parasitic silicon substrate under the buried oxide layer removed) will operate at higher temperatures (above 300°C). To further increase the temperature range while reducing MOS control, one should employ fully depleted (FD) MOSFET heaters built in ultra-thin SOI technology. The FD MOSFETs offer a better protection against the parasitic bipolar and hence can reach temperatures of up to about 400°C [14].

The sensitivity of the chemoresistor and the microcalorimeter to combustible gases is highly dependent on the sensing material used and the thermal properties of the membrane. In the case of the microcalorimeter we assumed,

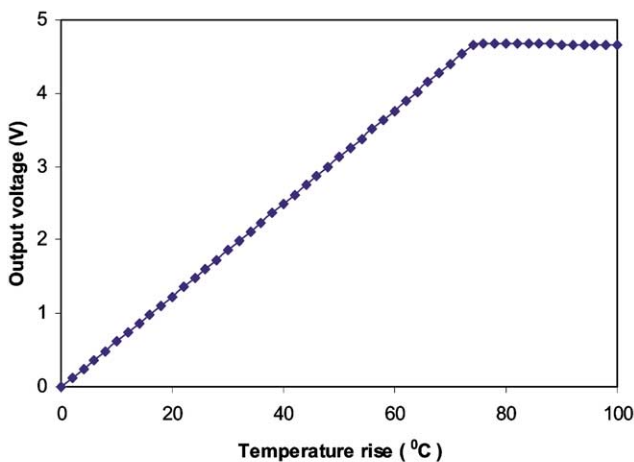

Fig. 11. Output voltage of the microcalorimeter transducer as a function of the temperature rise in the active cell due to the presence of a gas with relative to the reference cell.

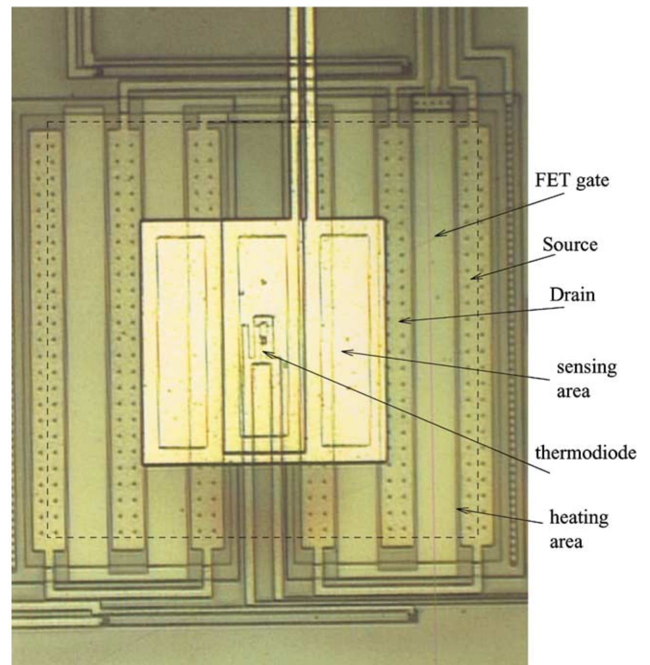

Fig. 12. A fabricated SOI gas sensor in relatively thick SOI technology.

as an exemplar, a required gas sensitivity of 5000 ppm of methane in air per degree centigrade [7]. The schematic circuit simulated with Spectre-S is shown in Fig. 5. A DC temperature analysis of the transducer has been carried out and the transducer output voltage as a function of the temperature difference between the active and the reference membrane is shown in Fig. 11. The differential amplifier was designed to have a high common mode rejection ratio (120 dB) and low DC offset. It used three operational amplifiers, each with two amplifying stages. The entire transducer was extracted from the layout and simulated. The net closed loop differential gain was adjusted to 32 dB. The input DC off-set voltage was found to be below 2 μV. This limits the minimum measurable input voltage drop to approximately 20 μV. Taking into account that up to 500 K, the forward-biased CMOS thermo-diode has a linear voltage drop/temperature characteristics with a gradient of approximately −2 mV/°C, the resolution (the minimum detectable gas concentration) of the sensor is estimated to be less than 50 ppm (methane in air) and the output sensitivity is 16 μV/ppm. The operating range of the differential amplifier (i.e. the maximum detectable difference between the temperature in the thermo-diode, in the active sensor, and that of the reference diode, before the output signal saturates), is ca. 75°C (Fig. 11). This allows detection and monitoring of a wide range of combustible gases, for instance from 50 to 375,000 ppm of methane in air. Note that the resolution and range of a metal oxide sensor is determined by the gas-sensitive layer and not by the heater.

6. Discussion and further work

Two sets of devices containing several prototypes of SOI smart gas sensors have been designed and are currently in fabrication. The two sets are fabricated on UNIBOND SOI wafers using the Europractice DMILL-Matra 0.8 μm double metal BiCMOS process with trench isolation. Two post-processing steps follow the standard BiCMOS process, namely (i) the deposition of an oxide layer using a droplet (micro-ink-jet) method for the chemoresistive sensor (or a catalyst for the microcalorimeter) and (ii) the single-sided back etching of the silicon substrate, using KOH. The first set, featuring *n*-channel MOSFET heaters and integrated thermo-diodes has passed the entire CMOS fabrication process and is currently undergoing the back-etch using KOH. The mask layer for the back-etch has been prepared and a PECVD nitride layer is used as an etch mask. The second set (batch), featuring *p*-channel MOSFET heaters, integrated thermo-diodes as well as new SOI-based poly-silicon and silicon heaters and spreading resistance temperature sensors is currently in progress at Matra Europractice. This batch also includes more advanced transducing circuits.

Fig. 12 shows a fabricated SOI gas sensor device, which can operate either as a chemo-resistive gas-sensor or as a microcalorimeter, depending on the sensing material deposited. It consists of a *n*-channel FET heater which occupies an area of 300 μm × 300 μm and a thermo-diode located in the centre. The device is placed in the centre of 500 μm × 500 μm membrane, which corresponds to a rear-side 1200 μm × 1200 μm etch area.

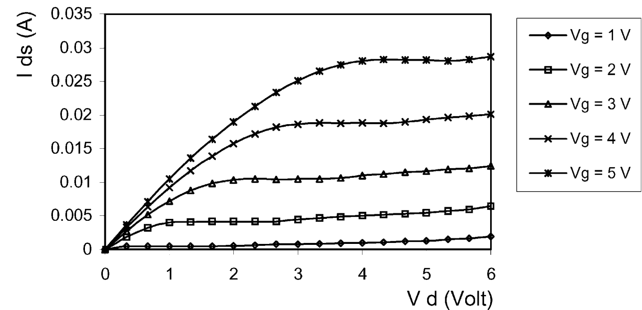

Fig. 13. The *I–V* characteristics of the SOI MOSFET heater prior to back-etching process.

The experimental *I–V* characteristics of the SOI MOSFET before back-etching of the substrate are shown in Fig. 13. The output voltage of the forward-biased SOI thermo-diode has a linear dependence with the temperature — with an experimental slope of −1.95 mV/°C. Further measurements will be carried out following the back-etching of the substrate and will be reported elsewhere together with full experimental results on the sensor and transducer behaviour at high temperatures in the presence of different combustible gases. Further work will also include a comparison between active and passive elements for the heater and temperature sensors in SOI CMOS-compatible technology. Finally, we will investigate the possibility of smart thermal modulation of the FET heater to either reduced the average power consumption of the device (pulsed mode) or enhance its chemical selectivity (cyclic mode) [20]. SOI MOSFET resistive or microcalorimeter gas sensor operated in this mode have enormous potential application within the field of battery-operated handheld gas monitors and, naturally, both multi-gas monitors and electronic "micro-noses" [21].

ISE takes into account the variation of the thermal conductivity of silicon with the doping level and temperature. This is done with a high accuracy, therefore we expect that the conduction losses quoted in this paper to be close to the true values. However, the convection coefficients have to be extracted more accurately from thermal measurements, to assess the full power losses of the sensors. Full thermal & electrical measurements of the SOI micro-hotplates will be reported elsewhere [22].

Finally, it may be necessary to ameliorate any possible piezoresistive effect when designing precision devices, e.g. PPM level sensitivity microcalorimeters. A piezoresistive effect, due to the strain induced in the membrane during bending, will affect the temperature measurement. In our device this is not anticipated to be a concern. Firstly, the diode can be placed close to the centre of the diaphragm (Figs. 3 and 12) where the strain is minimal. Secondly, the

junction lies close to the central (neutral) axis through the membrane. Thirdly, when operating the sensors in a differential mode, as shown in Fig. 5, the effect can be obviated. Because in this case the reference and the active membranes will undergo the same deflection and therefore will be subject to the same strain during high temperature operation. The variation in the voltage drop of the diode due to the strain and the absolute temperature is removed by using a comparator with a high common mode rejection ratio.

7. Conclusions

A new class of high temperature resistive gas sensors based upon a micro-hotplate SOI structure with a self-heating MOSFET is proposed. Our design is completely compatible with a standard CMOS/BiCMOS SOI process, that permits the integration of control and signal conditioning on the same silicon chip and, thereby, enables volume production at a relatively low unit cost.

We have carried out a comprehensive set of 2D & 3D numerical thermal and electrical simulations to design this new generation of sensors. Spectre-S analogue device and circuit simulations using a direct extraction of components (including parasitic elements) from the final Cadence layout have also been performed in order to asses accurately the performance of the heater, thermo-diode and the transducer.

The SOI smart sensors can operate at temperatures of up to 350°C, and yet offer excellent uniform thermal distribution over the sensing area and have the added advantage of simple temperature control via the applied gate voltage. The power consumption of this type of device is estimated to be below 100 mW, which is significantly lower than existing commercial resistive gas sensors and pellistors. Further simulations have shown that this design could have an integrated temperature sensor within the sensing area that permits accurate temperature monitoring of the FET heater without affecting significantly the temperature profile. Finally, we proposed two types of MOSFET micro-heater gas sensors based on SOI CMOS technology namely the chemo-resistive and microcalorimeter sensors.

Acknowledgements

This work is supported by the Engineering and Physical Science Research Council (EPSRC Grant Award GR2542). F. Udrea acknowledges the award of an advanced research fellowship from EPSRC — AF/100027.

References

[1] I. Ihokura, J. Watson, The Stannic Oxide Gas Sensor, CRC Press, Boca Raton, 1994.
[2] J.W. Gardner, A. Pike, N.F. de Rooij, M. Koudelka-hep, P.A. Clerc, A. Hierlemann, W. Goepel, Integrated array sensor for detecting organic solvents, Sens. Actuators B 26/27 (1995) 135–167.
[3] U. Dibbern, A substrate for thin-film gas sensor in microelectronic technology, Sens. Actuators B 2 (1990) 63–67.
[4] V. Demarne, A. Grisel, An integrated low-power thin-film CO gas sensor on silicon, Sens. Actuators B 4 (1991) 539–543.
[5] P. Krebs, A. Grisel, A low power integrated catalytic gas sensor, Sens. Actuators B 13/14 (1993) 155–158.
[6] M. Gall, The Si planar pellistor array, a detection unit for combustible gases, Sens. Actuators B 15/16 (1993) 260.
[7] M. Zanini, et al., Fabrication and properties of Si-based high-sensitivity microcalorimetric gas sensor, Sens. Actuators A 48 (1995) 187.
[8] J. Suehle, R. Cavicchi, M. Gaitan, S. Semancik, Tin oxide gas sensor fabricated using CMOS micro-hotplates and in situ processing, IEEE Electron Dev. Letts. 14 (3) (1993) 118–120.
[9] M.A. Gajda, H. Ahmed, J. Dodgson, CMOS-compatible silicon devices on thin SiO_2 membranes, Electron. Lett. 30 (1) (1994) 28–29.
[10] M.A. Gajda, H. Ahmed, Applications of thermal silicon sensors on membranes, Sens. Actuators A 49 (1995) 1–9.
[11] D. Briand, B. van der Schoot, N.F. de Rooij, H. Sundgren, I. Lundstrom, A low-power micromachined MOSFET gas sensor, J. Microelectromech. Syst. 9 (3) (2000) 303–307.
[12] F. Udrea, J.W. Gardner, Smart MOSFET gas sensor, British Patent GB2321336A, November 1996 and World Patent WO98/32009.
[13] J.W. Gardner, F. Udrea, W.I. Milne, Numerical simulation of a new generation of high-temperature, micropower gas and odour sensors based on SOI technology, in: Proceedings of the SPIE Smart Electronics and MEMS, Newport Beach, USA, 1–5 March 1999, pp. 104–112.
[14] J.P. Colinge, Silicon on Insulator Technology, Kluwer Academic Publishers, Dordrecht, 1991.
[15] ISE TCAD, Integrated Systems Engineering AG, Zurich, Switzerland.
[16] S. Astie, A.M. Gue, E. Scheid, L. Lescouzeres, A. Cassagnes, Optimization of an integrated SnO_2 gas sensor using a FEM simulator, Sens. Actuators A 69 (1998) 205–211.
[17] C.C. Lu, D. Setiadi, F. Udrea, W.I. Milne, J.A. Covington, J.W. Gardner, 3D Thermo-electro-mechanical simulations of gas sensors based on SOI membranes, Modeling and Simulation of Microsystems (MSM 2000), San Diego, pp. 297–300.
[18] C. Gotz, E. Cane, E. Lora-Tamayo, Specific problem of FEM thermal simulation for microsystem, in: Proceedings of the MicroSIM'95, Southampton, September 1995.
[19] A.C. Pike, J.W. Gardner, Thermal modelling and characterisation of micropower chemoresistive silicon sensors, Sens. Actuators B 45 (1997) 19–26.
[20] A. Heilig, N. Barsan, U. Weimar, M. Schweizer-Berberich, J.W. Gardner, W. Gopel, Gas identification by modulating temperature of SnO_2-based thick film sensor, Sens. Actuators B 43 (1997) 45–51.
[21] J.W. Gardner, Microsensors: Principles and Applications, Wiley, Chichester, 1994.
[22] J.W. Gardner, J.A. Covington, F. Udrea, T. Dogaru, C-C. Lu, W.I. Milne, Technical Digest of Transducers 01, Munich, 10–14 June 2001.

Biographies

Florin Udrea is a lecturer in Engineering Department at Cambridge University and since August 1998 an advanced EPSRC fellow. He completed his MSc degree in 1992 at Warwick University in solid-state gas sensors and his PhD at Cambridge University in 1995 in power devices. He initiated work on SOI devices at Cambridge University in 1996 to investigate and fabricate novel SOI power devices in CMOS-compatible technology. Dr. Udrea has actively been involved in design of micro-sensors for gas analysis and has published over 60 papers in journals and

international conferences and holds 13 patents in power semiconductor devices and sensors.

Julian W. Gardner (F'97) was born in Oxford, UK in 1958. He received a BSc with first class honours in 1979 from Birmingham University, a PhD from Cambridge University in 1983 on electron conduction in thin film devices, and a DSc from Warwick University in 1997 on electronic nose instrumentation. From 1983 to 1987 he was in industry where he worked on instrumentation and sensors. He is Professor of Electronic Engineering in the School of Engineering at Warwick University. His research interests include the modelling of electron devices, silicon microsensors, chemical sensor array devices and electronic noses. He is author or co-author of over 200 technical papers and patents as well as five technical books.

Dadi Setiadi obtained his MSc degree in 1991 from Delft University of Technology, The Netherlands. In 1995, he received the PhD degree in electrical engineering at University of Twente, The Netherlands. Since 1996 he has been with the Sensor System Group, Napier University, UK. He was working on the development of low-cost infrared system. In 1999, he became a research associate in Engineering department, Cambridge University, UK. His current research lies in the field of solid state sensors, silicon on insulator technology, and high temperature silicon sensors and circuits.

James Covington has graduated with a B.Eng. in Electronic Engineering from Warwick University in 1997. He is currently in his final year of his PhD at Warwick University. His interests are in FET-based silicon microsensors and smart sensors.

T. Dogaru has graduated with an MSc from the Poitehnica University of Bucharest in 1994. He is currently in the final year of his PhD at Charlotte University and has been a research associate at Cambridge University for the last 6 months. His interests are in magnetic and gas sensors and VLSI technology and circuits. He has published several papers in these fields and holds two patents on magnetic-type sensors.

Chih-Cheng Lu received his bachelor and master degrees in mechanical engineering from National Sun Yat-Sen University and National Chung-Hsing University, Taiwan, in 1989 and 1994, respectively. He was an assistant researcher working on precision engineering and MEMS at Precision Instrument Development Centre (PIDC), Taiwan, from 1994 to 1998, and was awarded Taiwan Governmental Scholarship in 1997. He is currently a PhD student at Engineering Department, Cambridge University, UK and studying in the fields of SOI gas sensors, micromachining and MEMS.

William I. Milne is a Professor of Electrical Engineering and has been Head of the Electrical Engineering Division in the Engineering Department at Cambridge University since October 1999. He also leads the Electronic Devices and Materials group within the department. This consists of approximately 40 people of whom 20 are PhD students and 10 are postdoctoral research workers. He has pioneered work on thin film amorphous materials and devices and his most recent interests include the production and application of amorphous and polycrystalline silicon films for large area electronics, diamond like carbon for electronic applications and smart power devices. He has published/presented approximately 350 papers in these and related topics and is an inventor on six patents.