Analog VLSI Design of an Adaptive Neuromorphic Chip for Olfactory Systems

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***Abstract*— In this paper, we present the analog circuit design and implementation of an adaptive neuromorphic olfaction chip. An analog VLSI device with on-chip chemosensor array, on-chip sensor interface circuitry and on-chip learning neuromorphic olfactory model has been fabricated in a single chip using Austria Microsystems 0.6 μm CMOS technology. Drawing inspiration from biological olfactory systems, the neuromorphic analog circuits used to process signals from the on-chip odour sensors make use of temporal "spiking" signals to act as carriers of odour information. An on-chip spike time dependent learning circuit is integrated to dynamically adapt weights for odour detection and classification. All the component subsystems implemented on chip have been successfully tested in silicon.**

I. Introduction

A neuromorphic olfactory chip attempts to mimic the powerful odour recognition features demonstrated by a biological olfactory system [1]. Previous works reported on implementing olfactory systems addressed: sensing [2], signal processing [3] and neuromorphic models [4], separately. Furthermore, implementations in digital hardware are inherently power hungry. An analog implementation of neuromorphic olfactory circuits benefits from low power, low cost and area efficient hardware realisations.

The neural circuits at the input stage of a mammalian olfactory system produce all-or-none action potentials or spikes occurring as temporal patterns [5]. In addition to the mounting biological evidence [6], it has been shown theoretically that temporal coding using individual spike times can produce powerful information processing systems [7]. Furthermore, recent experiment studies have shown that precise timing of spikes generated by neurons can be critical for the direction and magnitude of synaptic weight changes; a phenomenon now termed as spike-time-dependent plasticity (STDP) [6]. Spike time dependent learning rules can be used to learn temporal delays with high precision and have been used to model auditory processing in the barn-owl [8] and to model vision systems [9].

In this paper, we present the analog VLSI design and implementation of an adaptive neuromorphic olfaction chip. The neuromorphic analog circuits implemented on chip make use of temporal spiking signals to act as carriers of odour information. An on-chip spike-time-dependent learning circuit is integrated for dynamic weight adaptation. Implementation of on-chip learning is crucial for the design of an integrated odour sensing system. This not only emulates the plasticity function found in biological neural systems but also provides a means to compensate for analog imperfections in the physical implementation and changes in the environment in which they operate. All the component subsystems implemented on the neuromorphic olfaction chip have been successfully tested in silicon.

II. Description of Adaptive Neuromorphic Model

A. Model Dynamics

A neuromorphic architecture with spike-time-dependent learning (Fig. 1(a)) is used to model the olfactory pathway. The neuromorphic network receives sensory signals from an array of chemosensors which transform the molecular chemical information of an odorant into electrical signals suitable for processing in analog circuitry. The chemosensor array consists of different sensor types tuned to respond to different chemical compounds [2]. Such a heterogeneous array has the potential to increase the selectivity in the olfactory pattern recognition task while mimicking the function of the mammalian olfactory system. Because the signals from sensors of the same type are fed forward through neural elements to one and only one principal neuron, the network forms a distinct modular structure, reminiscent of the glomerular organisation of the mammalian olfactory bulb model [5].

The soma of each neuron element is modelled as a leaky integrate and fire (IF) unit. Below a threshold V_{th} the dynamics of the membrane potential $V_m(t)$ of the IF neuron is defined by

$$\frac{dV_m(t)}{dt} = -\frac{V_m(t) - V_{rest}}{R_m C_m} + \frac{I(t)}{C_m} \quad (1)$$

where t is time, R_m and C_m are respectively, the membrane resistance and capacitance, and $I(t)$ is the total input current to the neuron. V_{rest} is the membrane resting potential. If the potential $V_m(t)$ reaches the threshold value V_{th} it is immediately reset to the after hyperpolarization value V_{ahp} and a spike is produced as output of the neuron.

When a spike reaches a synapse, it induces a dendritic current that is fed into the post-synaptic neuron which decays exponentially with a characteristic time-constant, starting from a peak value determined by the synaptic weight. The sign

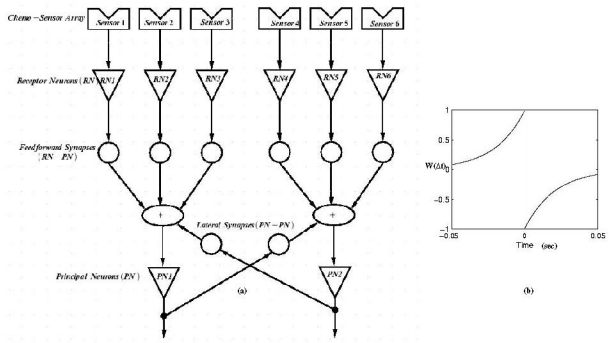

Fig. 1. (a) Neuromorphic architecture of olfactory pathway with STDP learning. (b) STDP learning window function.

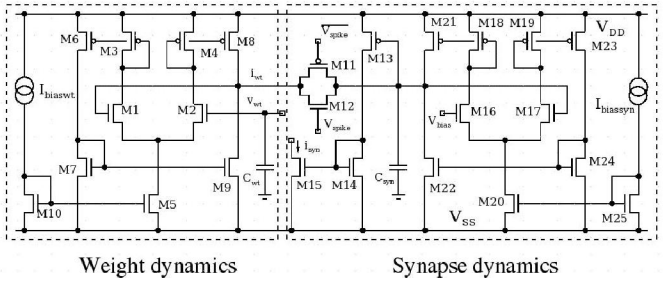

Fig. 2. Synapse Circuit

of the current is formally included into the synaptic weight, positive or negative according to whether the interaction is respectively, excitatory or inhibitory. If $t = 0$ is the instant in which the spike from a presynaptic neuron A reaches the synapse of A onto postsynaptic neuron B, the current evoked onto B by this single event is given by

$$i_{BA}(t) = \Theta(t) w_{BA} exp^{\frac{-t}{\tau_d}} \tag{2}$$

where $\Theta(t)$ is the Heaviside function and τ_d is a synaptic time constant. The total current induced by several presynaptic spikes by neuron A onto postsynaptic neuron B is given by

$$I_{BA}(t) = \sum_n i_{BA}(t - t_n) \tag{3}$$

where n indexes the spikes that are emitted by neuron A and reach the synapse at times t_n. If a neuron receives the outputs of several synapses, the respective contributions to the total post-synaptic current sum linearly. The total post-synaptic current constitutes the term $I(t)$ in Eq. 1, from which the membrane potential of the respective neuron is derived.

B. Weight Adaptation

In the neuromorphic model implemented, the network learns odorant features by modifying weights of the synapses according to a temporally asymmetric STDP rule [6]. The STDP, observed in biology, exhibits two characteristic properties. First, they are temporally asymmetric. Second, plasticity depends on timing of the spike within a learning time window. A biologically observed learning window function for spike-time-dependent plasticity is shown in Fig. 1(b). The learning window function for weight adaptation is defined as follows,

$$W(\Delta t) = \begin{cases} A_+ exp(\frac{(-\Delta t)}{t_{ln+}}) + A_{rest+} & \text{if } \Delta t > 0 \\ -A_- exp(\frac{(\Delta t)}{t_{ln-}}) - A_{rest-} & \text{if } \Delta t \leq 0 \end{cases} \tag{4}$$

where $\Delta t = t_{post} - t_{pre}$, is the time delay between postsynaptic neuron firing t_{post} and presynaptic firing t_{pre}. The learning window has two phases: a positive phase of synaptic potentiation for negative Δt and a negative phase of synaptic depression for positive Δt. The dynamics of the positive phase are generated by the arrival of an input spike at the synapse. The positive phase exhibits an exponential response with an initial amplitude of A_+ and decays to its resting level A_{rest+}. However, the dynamics of the negative phase are generated by the arrival of the postsynaptic neuron spike. This negative phase exhibits an exponential response with an initial amplitude of negative A_- decaying to its resting level A_{rest-}.

III. Neuromorphic Circuit Implementation

A. Synapse Circuit

The synaptic circuit is shown in Fig. 2. The circuit consists of a weight dynamics block and a synapse dynamics block. The input to the synapse is a presynaptic spike which triggers the injection of an incremental charging/discharging weight current into the synaptic capacitor C_{syn}. The incremental charging/discharging current is proportional to the capacitor weight voltage V_{wt}. The transistors M16-M24 form a balanced Operational Transconductance Amplifier (OTA). As the output of the OTA is fed back to the inverting input, output current is proportional to the voltage difference between the output and the input thereby acting as a resistor. The synaptic response is an exponentially decaying current and the output currents from various synapses are summed at the neuronal input.

The design of analog circuits with large time constants is critical for the implementation of a neuromorphic olfaction chip. This is because the chemical sensors have large time constants, typically in the order of 100 ms or more [2], which translates into large time constant requirements for the neuron and synapse models. In the design implemented on chip, large time constants are achieved by reducing the transconductance of the OTA stage thereby alleviating the need for implementing large area capacitors [10]. The transconductance reduction in the OTA stage is achieved by using large current mirror ratios. Noting the transconductance of an OTA is proportional to the ratio of the size of the output current mirrors (M22/M24) a multiplication of time constant by this ratio can be obtained. The advantage of this approach is that subthreshold currents exist in the output stage transistors (M21, M22) while all other transistors of the synapse dynamics circuit operate in the strong inversion region. The offset voltage of this OTA

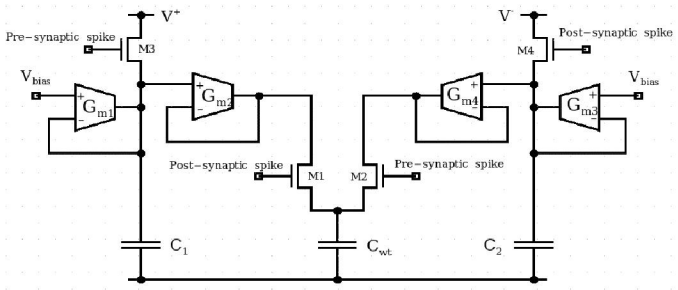

Fig. 3. Simplified schematic of the STDP learning circuit

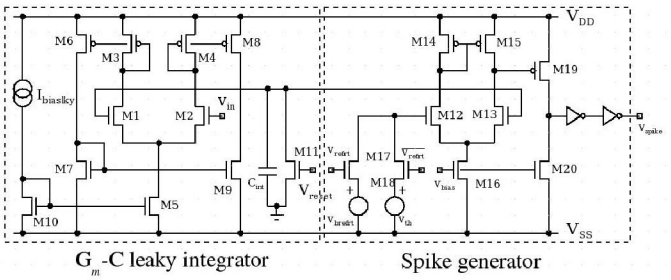

Fig. 4. Neuron Circuit

resistor is thus primarily determined by the leakage currents in the output node. The larger biasing currents in the OTA input transistors result in a larger linear range with reduced offset mismatching in layout. A programmable time constant can be achieved by using different dimension ratios at the output current mirror branch.

B. On-chip STDP Learning Circuit

In STDP learning, the relative time interval between the postsynaptic neuron firing and the presynaptic spike occurrence determines the weight change at the capacitor C_{wt}. Each synapse has an STDP based on-chip learning circuit associated with the weight storage capacitor. The component C_{wt} in Fig. 2 is the same as the component C_{wt} in Fig. 3.

The circuit uses two identical circuit blocks to define the negative phase and the positive phase of the learning window function. The weight adaption during the negative phase of the learning window function operates as follows. A presynaptic spike occurrence turns transistor M3 ON charging the capacitor C_1 to V_+. The trailing edge of the presynaptic spike switches the transistor M3 OFF and the voltage at the capacitor C_1 decays exponentially to a resting potential defined by V_{bias}. On the arrival of a postsynaptic spike, the transistor M1 is switched ON and the weight voltage at the capacitor C_{wt} is incremented by an amount proportional to the voltage at capacitor C_1 at that instant. Similarly, during the positive phase, a postsynaptic spike triggers an exponential response at capacitor C_{wt} and a following presynaptic spike decrements the weight at C_{wt}. The weight voltage at C_{wt} is strengthened, if the presynaptic spike precedes the postsynaptic arrival and weakened if the presynaptic spike follows the postsynaptic occurrence.

The STDP learning we have implemented is a dynamic learning mechanism and weight voltages stored on C_{wt} will decay if not refreshed. Long term weight storage can be performed by storing the weight voltage stored on C_{wt} in a non-volatile memory. The on-chip neuromorphic circuits are implemented in full analog unlike the previously reported implementations [11] that included digital circuits.

C. Neuron Circuit

A circuit schematic of the integrate and fire neuron is shown in Fig. 4. The leaky integrator dynamics (Eq. (1)) is implemented using an OTA-C circuit. Transistors M1-M7 form an OTA and C_{int} is the integrating capacitor. A two stage comparator circuit compares the output of the leaky integrator against a threshold V_{th}. The control signals V_{reset} and V_{refrt} are the outputs of the reset timer and refractory period timer circuits respectively which are both implemented using comparators and OTA-C delay circuits (not shown).

Initially the V_{reset} and V_{refrt} signals are at a low state. The comparator output V_{spike} goes high when the leaky integrator response is above a threshold V_{th}. The leading edge of the neuron spike activates the reset and refractory period timers circuits. The reset timer output V_{reset} goes high after a finite time interval which in turn resets the integrating capacitor C_{int} causing the neuron output to go low. The trailing edge of V_{spike} triggers the refractory timer V_{refrt} to a high state. The control signal V_{refrt} switches the comparator threshold V_{th} to a large voltage V_{brefrt} thereby inhibiting the neuron from firing. However, the leaky integrator continues to integrate during the refractory period. The time delay of the reset timer and refractory period circuit timer determines the pulse width of the neuron spike and the refractory period, respectively.

IV. Chip Results

The architecture of the fabricated chip implements a slice of the network in Fig. 1(a) such that a scalable olfactory system can be constructed by interconnecting multiple chips. The chemosensors in the chip are separated by a distance of 1.2 mm. Each sensor cell has an associated sensor interface circuit for DC cancellation, amplification and filtering. The outputs of sensor interface circuits feed to the inputs of the neuromorphic circuits. The die area of the chip is 50 mm^2 with a core circuit area of 6.5 mm^2, i.e. the chip is pad limited.

The working of the chemosensor array and its interface circuitry had been previously implemented and tested on a separate chip prior to integrating in this chip [12]. The chemosensors are coated with five different carbon black polymers [2]. Fig. 5(a) shows the response characteristics of the chemosensors to ethanol vapour in air when tested at a flow rate of 25 ml/min and pulse width of 5 s at room temperature (25 ^{o}C $\pm$ 2 ^{o}C, 40 % $\pm$5 % R.H.). The response magnitudes and profiles are distinct to different sensor types in the array. Transient sensor information is extracted at the neuromorphic circuit stage to aid the discrimination and classification of the

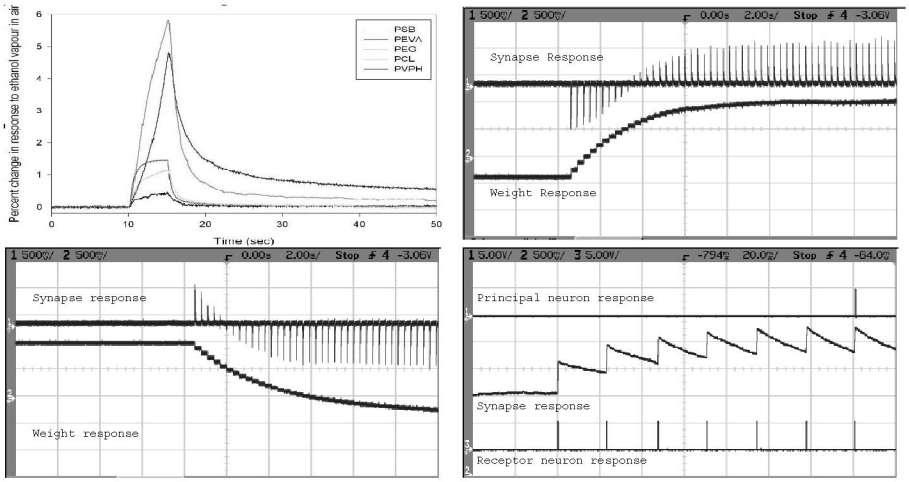

Fig. 5. Measured Chip Results: (a) Sensor response characteristics to ethanol vapour in air. (b) Weight strengthening during on-chip STDP learning. (c) Weight weakening during on-chip STDP learning. (d) Network response showing the dynamics of the receptor neuron, synapse and principal neuron.

input odour.

The performance of the on-chip adaptive neuromorphic circuits are evaluated in silicon. The spike-time-dependent learning circuit implemented on chip is tested under different presynaptic and postsynaptic input spike conditions. Fig. 5(b) shows the measured on-chip learning response when excited by a presynaptic spike preceding the occurrence of a post synaptic spike by 5 ms. Initially, the synaptic weight is negative causing the synapse to generate an inhibitory response. As the presynaptic spikes arrive prior to the occurrence of postsynaptic spikes, the weights are strengthened and the synaptic response becomes excitatory as shown in Fig. 5(b). Fig. 5(c) shows the synaptic response and weight dynamics when presynaptic spikes follow the occurrence of postsynaptic spikes by 5 ms. As the presynaptic spikes arrive after the occurrence of postsynaptic spikes, the synapse response do not contribute to the firing of the postsynaptic neuron. Hence the weights are weakened and the synapse response becomes inhibitory. The weight increment (decrement) is smaller if the presynaptic spike and precedes (follows) the postsynaptic spike by a larger time interval. Fig. 5(d) shows the dynamics of the receptor neuron, synapse and principal neuron in a network. The receptor neuron fires at a rate of approximately 25 ms. The exponential synaptic current increases causing the principal neuron to fire once. The maximum weight range of the circuit is found to be ± 1 V on a ± 2.5 V power supply range.

V. Conclusion and Future Work

A prototype analog VLSI chip with an on-chip chemosensor array, on-chip sensor interface circuitry and on-chip STDP olfactory bulb model has been fabricated using 0.6 μm CMOS technology. All the component subsystems implemented on chip have been successfully tested in silicon. The next step is to integrate and test the prototype chip with an odour delivery system.

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