UNIVERSITY OF
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Novel Silicon Tracker Technologies for the HL-LHC and beyond

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Particle Physics Seminar, University of Warwick

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Outline

- Introduction to silicon detectors with examples from state-of-the-art technology
- Challenges for future tracking detectors and R&D roadmap
- CMOS sensors
- 4D tracking
- Conclusion

Segmented silicon detectors

- Highly segmented silicon detectors are the technology of choice for vertex and tracking detectors at collider experiments

- They detect the passage of ionizing radiation with good spatial resolution and efficiency in the harsh experimental conditions close to the interaction point

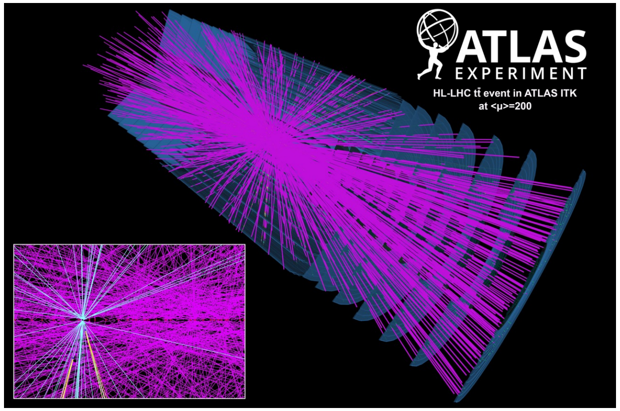
- Different types of silicon detectors exists to satisfy a range of requirements in terms of spatial resolution, radiation hardness, data rate, area, material budget, etc. at different experimental conditions

- Technologies for high occupancy, high radiation environments
    - Example: hybrid pixel detectors and strip detectors for the ATLAS ITk

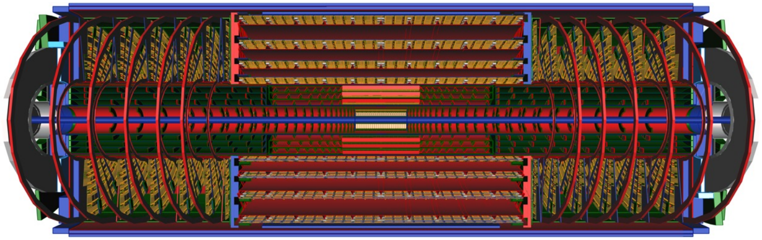
- Technologies for extremely precise tracking systems
    - Example: monolithic active pixel sensors for ALICE ITS2

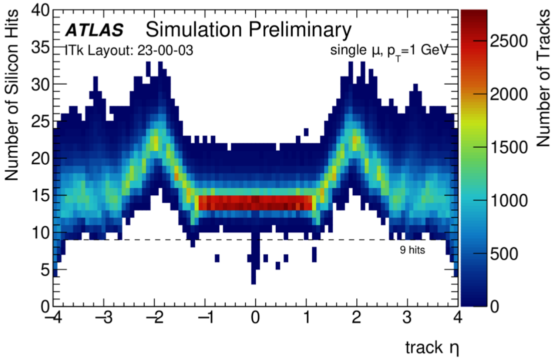
ATLAS Inner Tracker at HL-LHC*

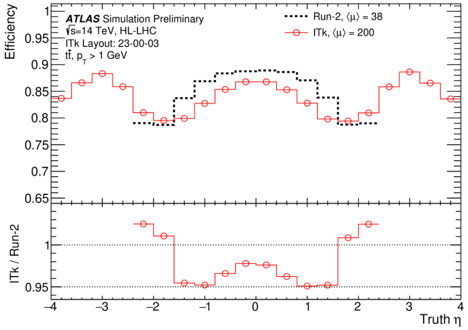
- The ATLAS ITk should have the same or better performance as the current detector but in the harsher environment of the HL-LHC
  - ⟨μ⟩ ~ 200 at 7.5×10^{34} $cm^{-2}s^{-1}$ peak luminosity
  - 4000 fb^{-1} integrated luminosity, fluences up to 2×10^{16} MeV n_{eq}/cm^2, TID up to 1 Grad



- New all-silicon detector designed using state-of-the-art silicon technologies optimised for operation in a high rate, high radiation environment
  - 13 m^2 of hybrid pixel detectors, 165 m^2 of strip detectors, 1-2% x/X_0 per layer
  - Extended coverage up to eta 4 with at least 9 space points per track







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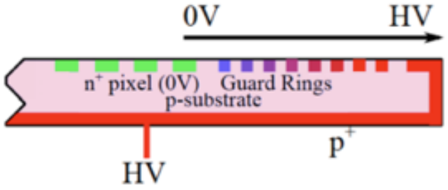
[*] The ATLAS and CMS experiments have completed R&D for their HL-LHC trackers upgrade and are starting detector production. Their upgraded trackers are thus considered state-of-the-art in this talk.

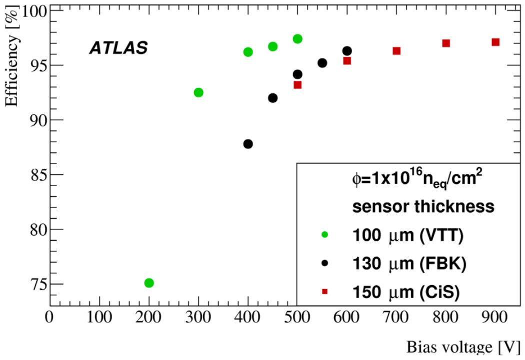
ITk pixel detector

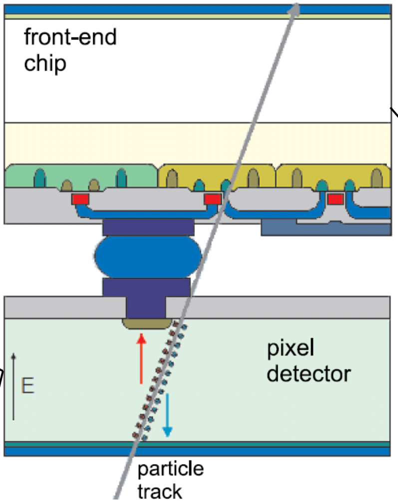
Hybrid pixel detectors: Currently the only technology that can cope with very high rate. Developed specifically for the LHC experiments. Sensor and FE are separate entities connected via fine pitch bump bonding.

Planar sensors

50x50 μm², 100-150 μm thin



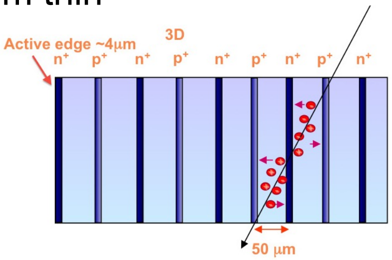


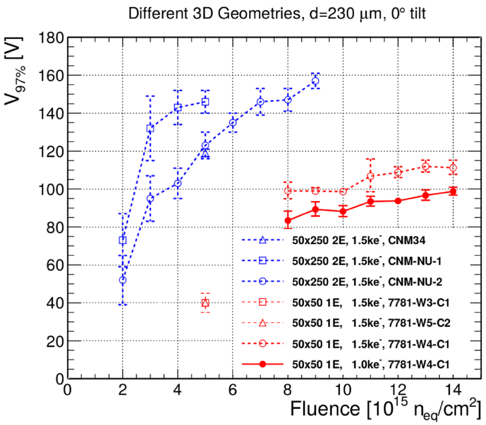


3D sensors

50x50 and 25 x 100 μm²

150 μm thin

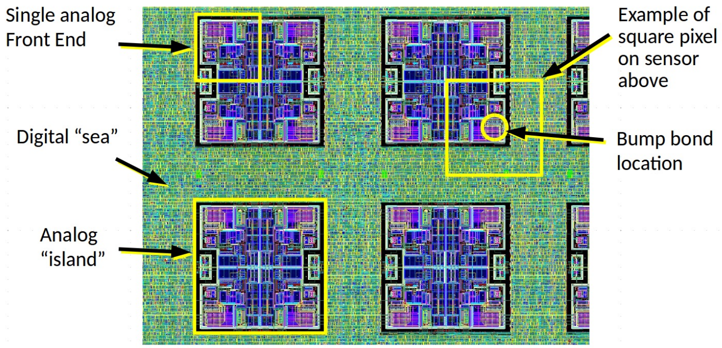




97% efficiency measured at test beams for fluence up to 1×10^{16} MeV n_{eq}/cm^2

FE chip

- Joint ATLAS CMS development (RD53)
- New technology node: 65 nm CMOS
- Innovative design based on a new readout architecture



Pixel size: 50x50 μm²

Hit rate: 3GHz/cm²

RO data rate: 5.12 Gbits/s

Rad tolerance 500Mrad at -15C

Power consumption <1W/cm²

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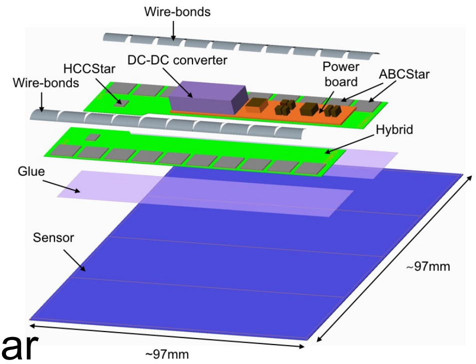
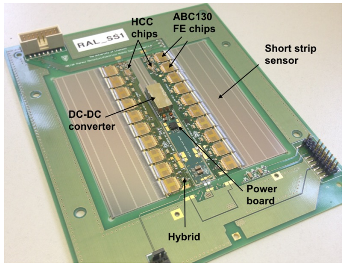
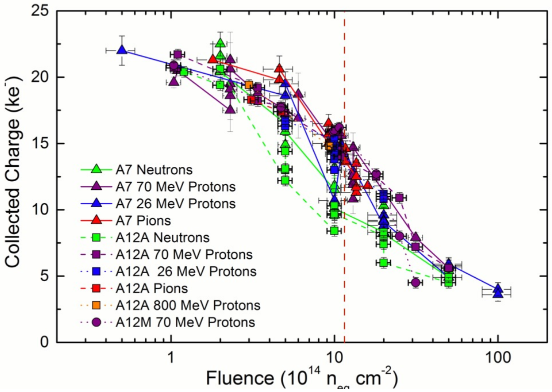
ITk strip detector

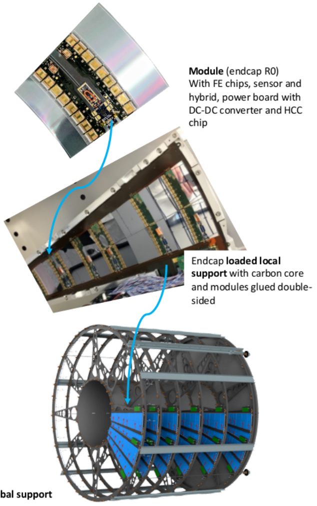




- ☐ Module = sensor + hybrid + powerboard
  - – Strip pitch 75 μm, thickness 300 μm
  - – Three dedicated 130 nm CMOS FE: ABCStar (readout), HCCStar (data aggregator), AMAC (power and T monitoring)
  - – Design compatible with multi-level trigger scheme



- ☐ Lower data rate and radiation levels but more challenging large area production
  - – Modularity of components for mass production
  - – Assembly and testing at multiple sites
  - – Industrialised production flow (common tooling and assembly procedures)
  - – Extensive QC/QA to assure reliability in extreme experimental conditions, monitor rate and quality of production
  - – Database to store QC/QA results and track components



Module (endcap R0)
With FE chips, sensor and hybrid, power board with DC-DC converter and HCC chip

Endcap **loaded local support** with carbon core and modules glued double-sided

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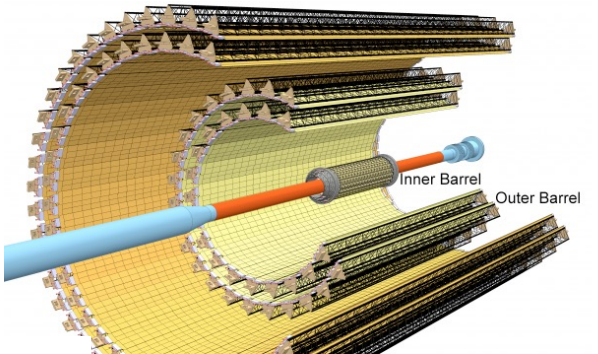
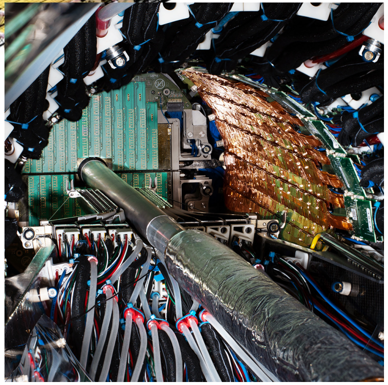
ALICE Inner Tracking System Upgrade (ITS2)

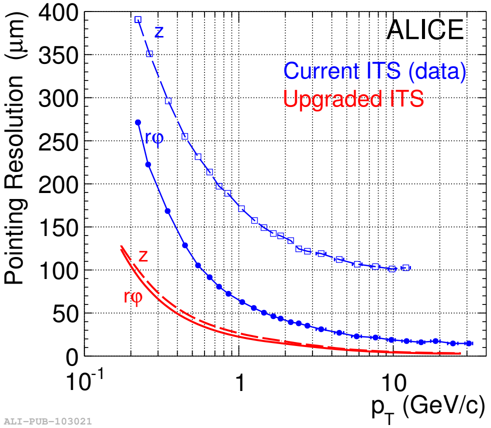


- First large-area silicon vertex detector based on the CMOS Monolithic Active Pixel Sensor (MAPS) technology optimised for extremely precise tracking
  - Sensor and electronics share the same silicon substrate
  - Small pixel pitch, very low material budget



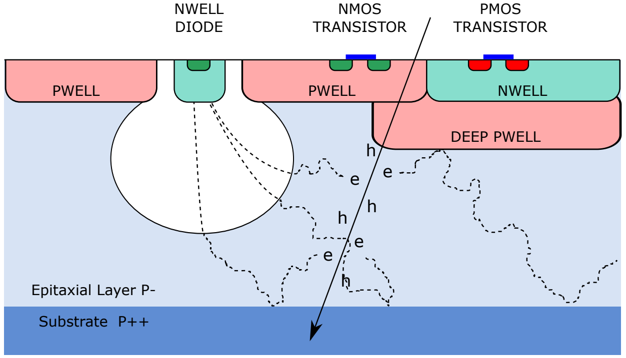
ITS2 vertex detector

7 layers, $10 m^2$, 12.5 G pixels
Innermost layer at r = 2.3 cm
Inner barrel: 0.3% x/X_0
Outer barrel: 0.8% x/X_0



ALPIDE sensor

180 nm TJ CMOS imaging technology
28 x 28 μm^2 pixel pitch, 50 - 100 μm thickness
Power density = 40 mW/cm^2
50 kHz interaction rate
<20 μs integration time
NIEL: 1.7×10^{13} 1 MeV n_{eq}/cm^2, TID: 2.7 Mrad



http://dx.doi.org/10.1016/j.nima.2015.09.057
https://arxiv.org/abs/2001.03042

Requirements for Vertex and Tracking Detectors

"Technical" Start Date of Facility (This means, where the dates are not known, the earliest technically feasible start date is indicated - such that detector R&D readiness is not the delaying factor)				**< 2030**					**2030-2035**					**2035 - 2040**	**2040-2045**		**> 2045**		
				Panda 2025	CBM 2025	NA62/Klever 2025	Belle II 2026	ALICE LS3 $^{1)}$	ALICE 3	LHCb (≳LS4)$^{1)}$	ATLAS/CMS (≳ LS4)$^{1)}$	EIC	LHeC	ILC $^{2)}$	FCC-ee	CLIC $^{2)}$	FCC-hh	FCC-eh	Muon Collider
Vertex Detector$^{3)}$	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.1 DRDT 3.4	Position precision σ_{hit} (μm)		≃ 5		≲ 5	≃ 3	≲ 3	≲ 10	≲ 15	≲ 3	≃ 5	≲ 3	≲ 3	≲ 3	≃ 7	≃ 5	≲ 5
			X/X_0 (%/layer)	≲ 0.1	≃ 0.5	≃ 0.5	≲ 0.1	≃ 0.05	≃ 0.05	≃ 1		≃ 0.05	≲ 0.1	≃ 0.05	≃ 0.05	≲ 0.2	≃ 1	≲ 0.1	≲ 0.2
			Power (mW/cm^2)		≃ 60			≃ 20	≃ 20			≃ 20		≃ 20	≃ 20	≃ 50			
			Rates (GHz/cm^2)		≃ 0.1	≃ 1	≲ 0.1		≲ 0.1	≃ 6		≲ 0.1	≃ 0.1	≃ 0.05	≃ 0.05	≃ 5	≃ 30	≃ 0.1	
			Wafers area (")$^{4)}$					12	12			12			12		12		12
		DRDT 3.2	Timing precision σ_t (ns)$^{5)}$	10		≲ 0.05	100		25	≲ 0.05	≲ 0.05	25	25	500	25	≃ 5	≲ 0.02	25	≲ 0.02
		DRDT3.3	Radiation tolerance NIEL (x 10^{16} neq/cm^2)							≃ 6	≃ 2						≃ 10^2		
			Radiation tolerance TID (Grad)							≃ 1	≃ 0.5						≃ 30		
Tracker$^{6)}$	MAPS Planar/3D/Passive CMOS LGADs	DRDT 3.1 DRDT 3.4	Position precision σ_{hit} (μm)						≃ 6	≃ 5		≃ 6	≃ 6	≃ 6	≃ 6	≃ 7	≃ 10	≃ 6	
			X/X_0 (%/layer)						≃ 1	≃ 1		≃ 1	≃ 1	≃ 1	≃ 1	≃ 1	≲ 2	≃ 1	
			Power (mW/cm^2)						≲ 100	≃ 100		≲ 100		≲ 100	≲ 100	≲ 150			
			Rates (GHz/cm^2)							≃ 0.16									
			Wafers area (")$^{4)}$						12			12		12	12	12	12		12
		DRDT 3.2	Timing precision σ_t (ns)$^{5)}$						25	≲ 25		25	25	≲ 0.1	≲ 0.1	≲ 0.1	≲ 0.02	25	≲ 0.02
		DRDT3.3	Radiation tolerance NIEL (x 10^{16} neq/cm^2)							≃ 0.3							≲ 1		
			Radiation tolerance TID (Grad)							≃ 0.25							≲ 1		

https://cds.cern.ch/record/2784893

Technology development

DRDT 3.1 - Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors.
Developments of Monolithic Active Pixel Sensors (MAPS) should achieve very high spatial resolution and very low mass, aiming to also perform in high fluence environments. To achieve low mass in vertex and tracking detectors, thin and large area sensors will be crucial. For tracking and calorimetry applications MAPS arrays of very large areas, but reduced granularity, are required for which cost and power aspects are critical R&D drivers. Passive CMOS designs are to be explored, as a complement to standard sensors fabricated in dedicated clean room facilities, towards hybrid detector modules where the sensors is bonded to an independent ASIC circuit. Passive CMOS sensors are good candidates for calorimetry applications where position precision and lightness are not major constraints (see Chapter 6). State-of-the-art commercial CMOS imaging sensor (CIS) technology should be explored for suitability in tracking and vertex detectors.

DRDT 3.2 - Develop solid state sensors with 4D-capabilities for tracking and calorimetry.
Understanding of the ultimate limit of precision timing in sensors, with and without internal multiplication, requires extensive research together with the developments to increase radiation tolerance and achieve 100%-fill factors. New semiconductor and technology processes with faster signal development and low noise readout properties should also be investigated.

DRDT 3.3 - Extend capabilities of solid state sensors to operate at extreme fluences.
To evolve the design of solid state sensors to cope with extreme fluences it is essential to measure the properties of silicon and diamond sensors in the fluence range $1\times10^{16}\,\mathrm{n_{eq}\,cm^{-2}}$ to $5\times10^{18}\,\mathrm{n_{eq}\,cm^{-2}}$ and to develop simulation models which correspondingly include results from microscopic measurements of point and cluster defects. All technologies will need improved radiation tolerance for use at future hadron collider experiments. Exploration of alternative semiconductors and 2D-materials should already start, having as a target full functionality even after the extreme fluences present in the innermost parts of the detectors. A specific concern to be addressed is the associated activation of all the components in the detector. Exploration is desirable on alternative semiconductors and 2D-materials to further push radiation tolerance.

DRDT 3.4 - Develop full 3D-interconnection technologies for solid state devices in particle physics.
3D-interconnection is commercially used, for instance in imaging sensors, to use the most appropriate technology process for the different functionalities of the devices. For particle physics detectors, this process would allow more compact and lighter devices with minimal power consumption. This approach also provides an alternative to the use of finer feature sizes to enable lower pitch and new digital features. An enhanced R&D effort towards building a demonstrator as a starting cornerstone is highly desirable. A demonstrator programme should be established to develop suitable silicon sensors, cost effective and reliable chip-to-wafer and/or wafer-to-wafer bonding technologies and to use these to build multi-layer prototypes with vertically stacking layers of electronics, interconnected by through-silicon vias (TSVs) and integrating silicon photonics capabilities.

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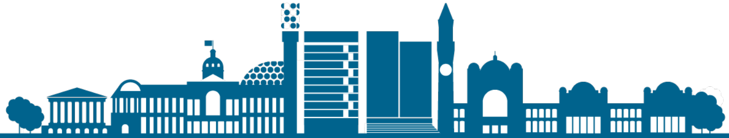
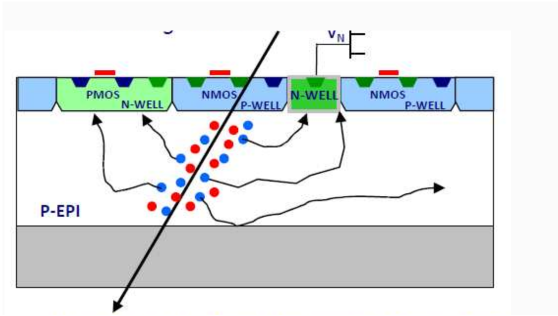


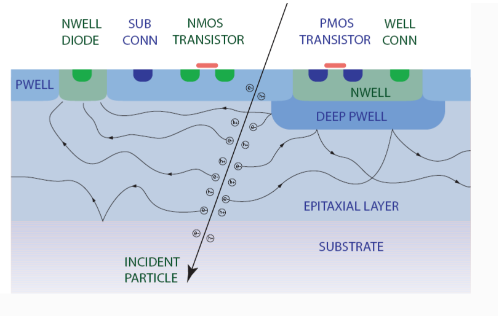
Monolithic Active Pixel Sensors

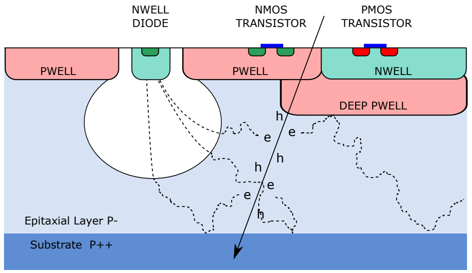
Monolithic active pixel sensors

- Traditional MAPS sensors deliver high spatial resolution through small pixel pitch and low material budget (i.e. low power consumption) and provide a simplified module concept wrt hybrids

- The ALPIDE has brought a breakthrough wrt to previous generations
  - It collects charge in part by drift → moderate rad-hard charge collection
  - It integrates full CMOS electronics → more in-pixel logic
  - It is fabricated in a commercial CMOS imaging process → low cost high volume production





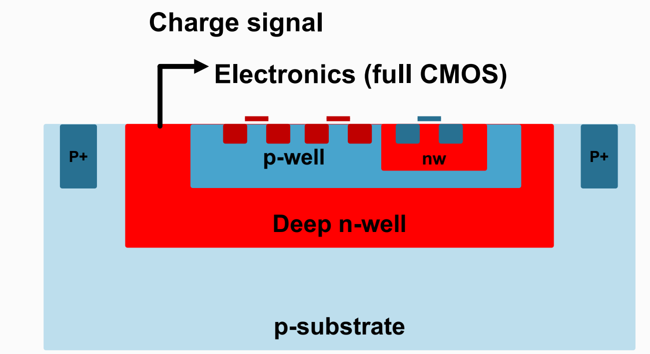


MAPS would be the perfect technology for large area trackers, but can they be made fast and radiation-hard?

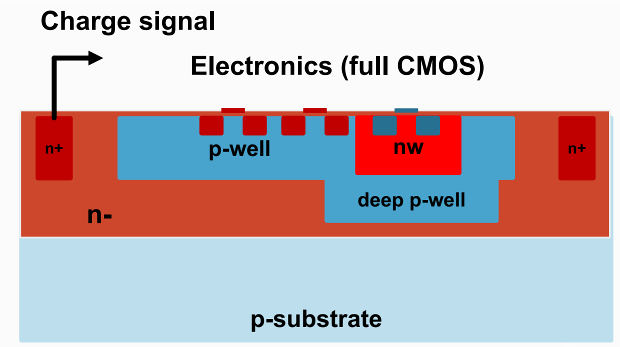
Depleted MAPS

- ☐ Fast and radiation hard charge collection requires a fully depleted sensor volume in which charges move by drift
- ☐ Need high resistivity substrates and/or being able to apply a high voltage to the sensor → This can be achieved with a number of CMOS imaging processes
- ☐ Need to achieve uniform depletion = uniform electric field → requires a change in the sensor design

Large collection electrode design



Modified small collection electrode design

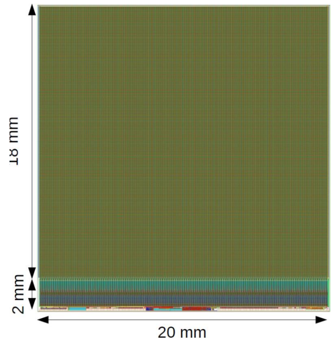


DMAPS prototypes

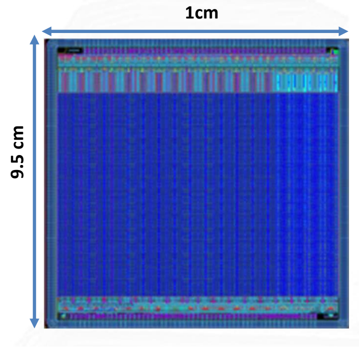
- ~ 10 years of developments led to mature prototypes of both structures that have demonstrated radiation hardness up to a few 10^{15} MeV n_{eq}/cm^2

Large collection electrode:

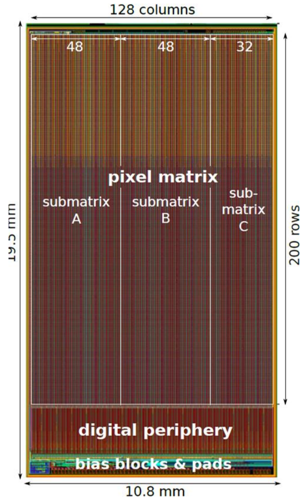
ATLASPix3 180 nm TSI



LF-MONOPIX 150 nm LFoundry

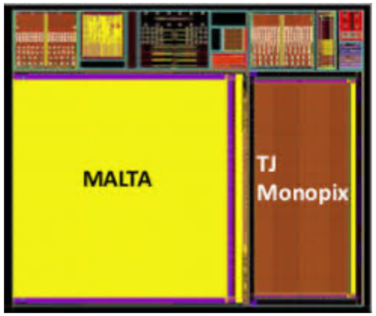


MuPix8 @ mu3e
180 nm AMS



Modified small collection electrode:

MALTA and TJ-MONOPIX
180 nm TowerJazz



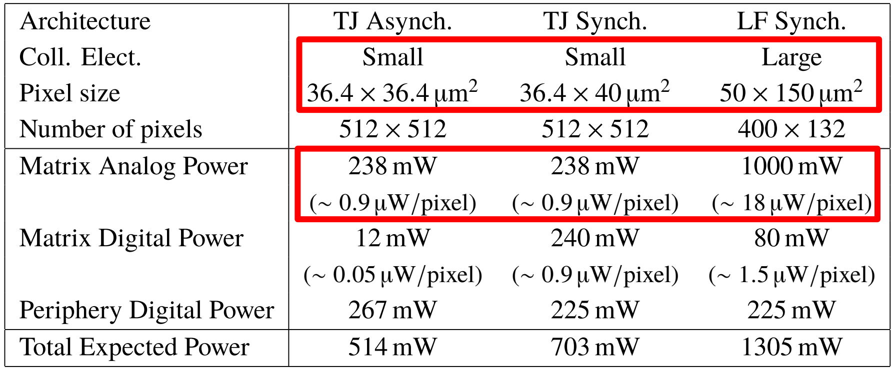
… and many more, see also ARCADIA project and RD50 developments

Small collection electrode development

- The small collection electrode design has a very small detector capacitance that allows to design a compact, low power FE → small pixels and low material
  - <5fC for small electrode vs. a few hundred fC for large electrode

Estimated power consumption of ITk full scale 2x2 cm² DMAPS

MALTA TJ-MONOPIX LF-MONOPIX



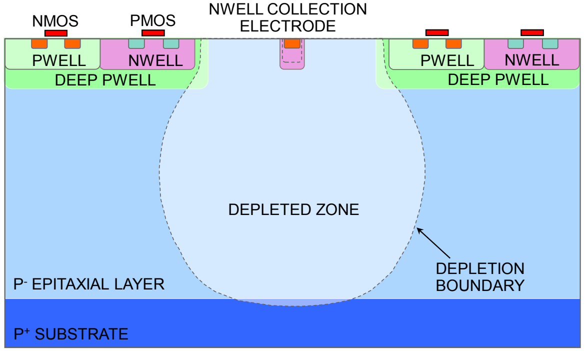
Architecture	TJ Asynch.	TJ Synch.	LF Synch.
Coll. Elect.	Small	Small	Large
Pixel size	$36.4 \times 36.4\,\mu m^2$	$36.4 \times 40\,\mu m^2$	$50 \times 150\,\mu m^2$
Number of pixels	512×512	512×512	400×132
Matrix Analog Power	238 mW (~ 0.9 µW/pixel)	238 mW (~ 0.9 µW/pixel)	1000 mW (~ 18 µW/pixel)
Matrix Digital Power	12 mW (~ 0.05 µW/pixel)	240 mW (~ 0.9 µW/pixel)	80 mW (~ 1.5 µW/pixel)
Periphery Digital Power	267 mW	225 mW	225 mW
Total Expected Power	514 mW	703 mW	1305 mW

https://doi.org/10.1088/1748-0221/14/06/C06019

- Radiation-hardness is challenging, significant effort to develop process modifications (CERN/TJ collaboration)
- Different readout architectures explored for low power readout at high rate
  - MALTA: novel asynchronous architecture
  - TJ-MONOPIX: synchronous column drain architecture

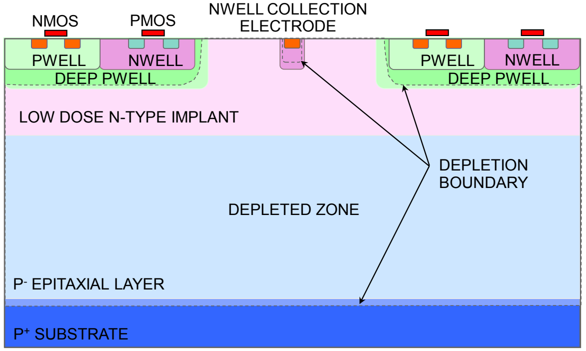
Modifications of small collection electrode design

Standard TJ 180 nm process
(as in ALPIDE)

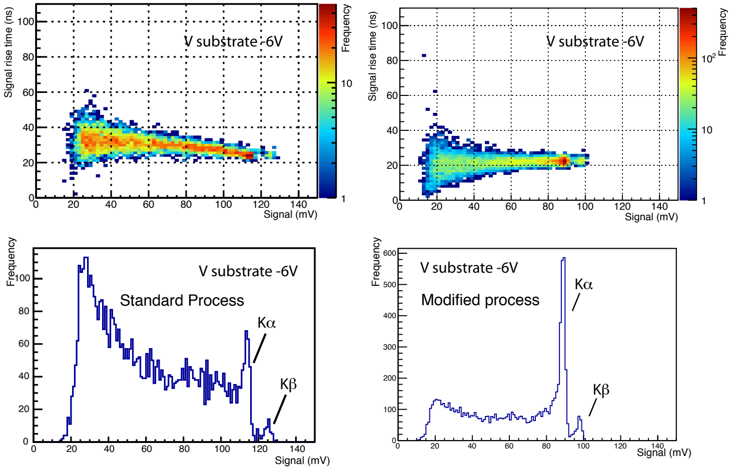


Add low dose n-implant to improve depletion under deep p-well

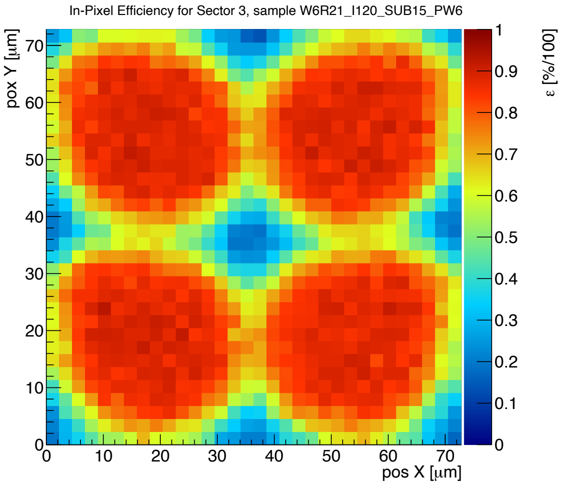
Modified TJ 180 nm process



Results on pixel test structures (TJ investigator) indicated larger depletion



Efficiency for the first MALTA prototype measured in a 180 GeV proton beam (2018) – Degradation at pixel edges after 10^{14} n_{eq}/cm^2

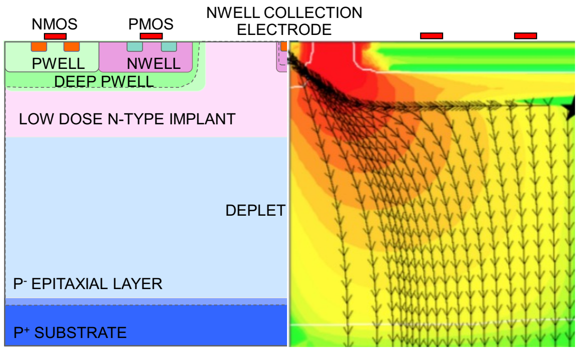


http://dx.doi.org/10.1016/j.nima.2017.07.046
https://doi.org/10.1088/1748-0221/14/05/C05013
https://doi.org/10.1016/j.nima.2019.162404

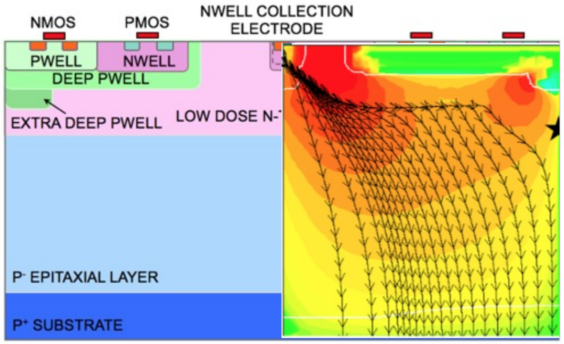
Modifications of small collection electrode design

- Further modifications needed to improve lateral field strength

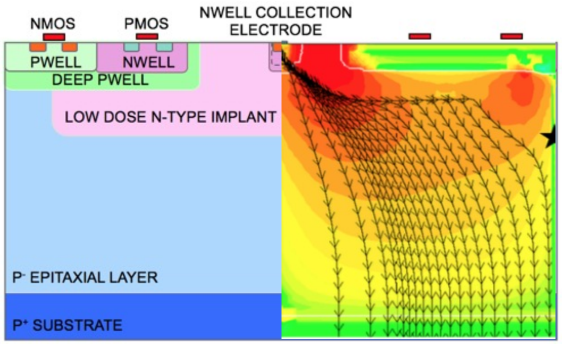
Modified



Modified extra deep pwell

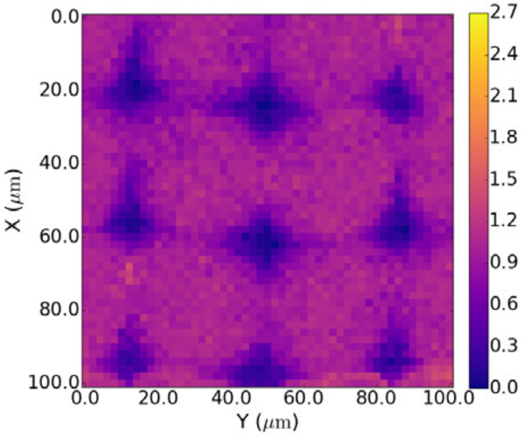


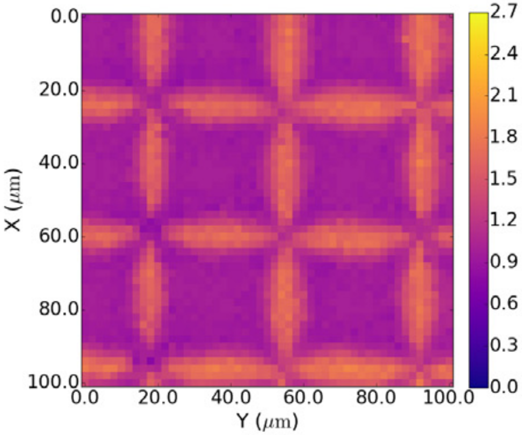
Modified n-gap

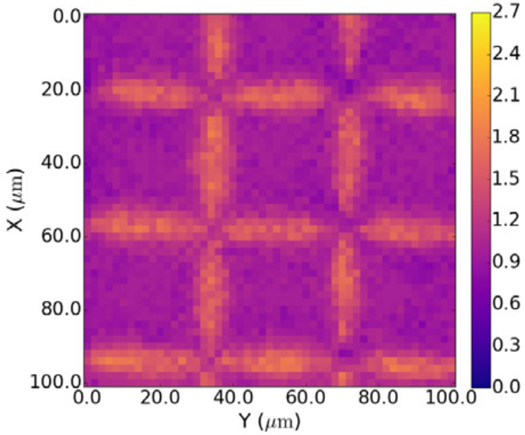


- Mini-MALTA pixel sectors with different sensor modifications tested with a x-ray beam at the Diamon Light Source (2019) demonstrate improved response at pixel edges after $1\times10^{15}\ n_{eq}/cm^2$

https://doi.org/10.1016/j.nima.2019.163381



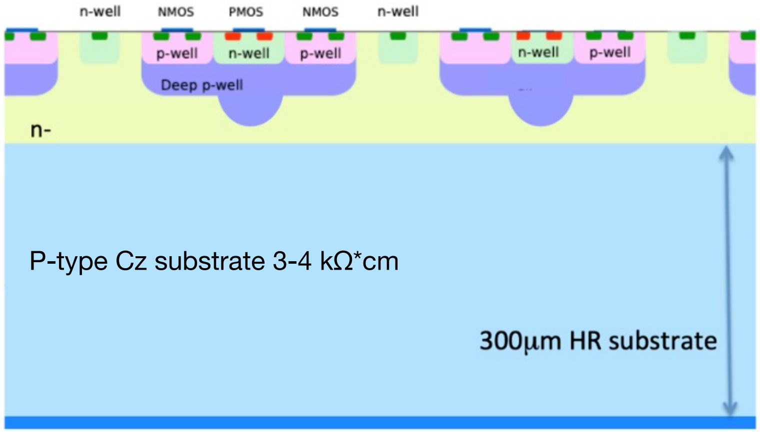


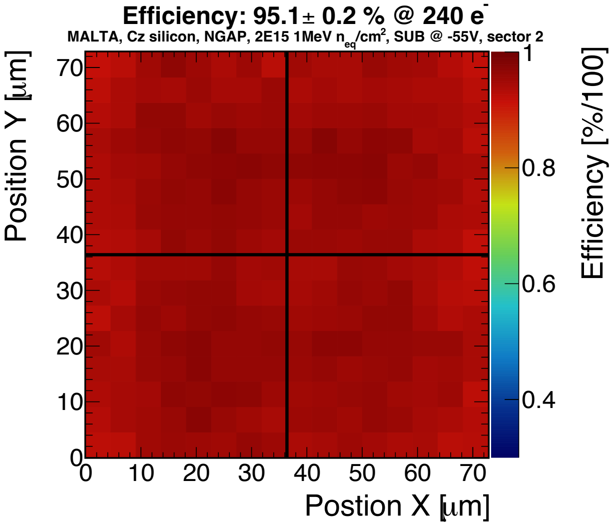


Modifications of small collection electrode design

- One of the most recent MALTA version has been implemented on high resistivity Czochralski substrate
  - Resistivity and bias voltage higher than for epitaxial layer in previous prototypes
  - Implemented with modified, n-gap, deep p-well modifications
  - Higher charge collection, time resolution, radiation hardness expected

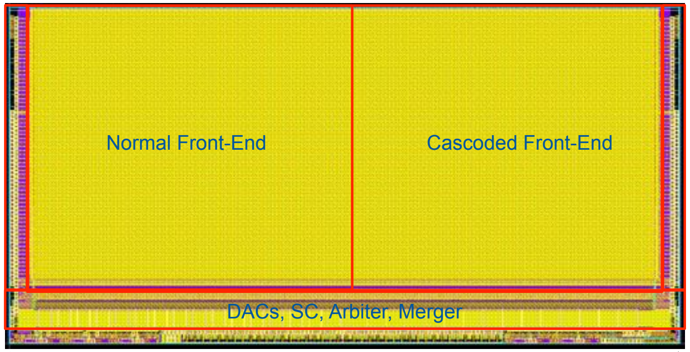
- MALTA Cz sensors allow further depletion than epitaxial layers
  - Corner efficiency after 2×10^{15} n_{eq}/cm^2 fully recovered with extra process modification measured at DESY test beam 4 GeV electron beam (2019)





https://indico.cern.ch/event/1047531/contributions/4521226/

Continuing MALTA programme



- MALTA2
  - Latest full-scale prototype
  - 20 x 10 mm^2 size demonstrator
  - 224 x 512 MALTA pixels
  - epi & Cz material
  - Best sensor layout for each material selected for production
  - Further FE improvements
  - 97.5% charge collection efficiency after 2E15 1 MeV n_{eq}/cm^2
  - More testing ongoing

- MALTA3
  - More focused on readout capabilities (timing performance, improved integration capabilities)
  - Design ongoing

https://indico.cern.ch/event/949529/attachments/2091301/3516122/The_MALTA_Sensor.pdf
https://doi.org/10.1016/j.nima.2022.167226

Next generation MAPS: 65 nm CMOS sensors

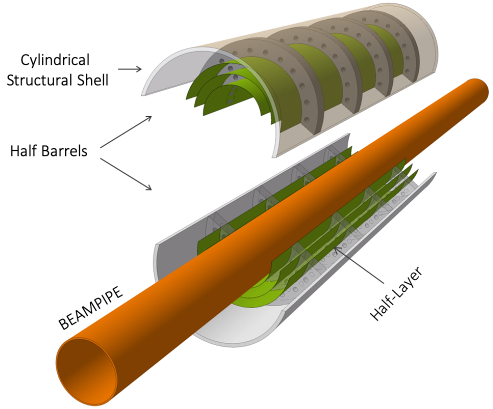
- DMAPS in 150/180nm CMOS imaging processes are approaching HL-LHC rate capability and radiation hardness
  - Candidates for ATLAS inner vertex layers replacement after 2030

- Future facilities present bigger challenges → explore smaller feature size technology

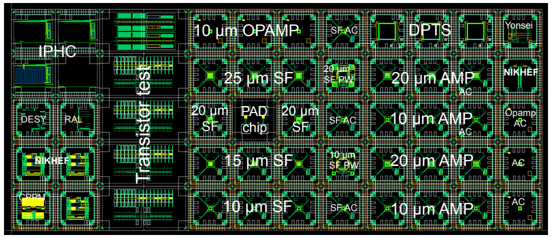
- R&D is starting to develop MAPS in 65 nm CMOS imaging process for use at future collider facilities
  - Higher logic density (increased performance/area, higher granularity)
  - Lower power
  - Higher speed (logic, data transmission…)
  - Process availability
  - Higher NRE costs and complexity, but lower price per area

Ongoing 65 nm R&D for ALICE ITS3 vertex detector

- New generation MAPS sensor at the 65 nm node to design a truly cylindrical, extremely low mass (0.05% x/X0) vertex detector (~0.12m^2) for the HL-LHC (after 2030)
  - Exploit stitching over large area to design wafer scale sensors
  - Thin sensors bent around the beam pipe
  - Lower power in 65 nm allows air cooling
  - Minimal support needed and services outside active area



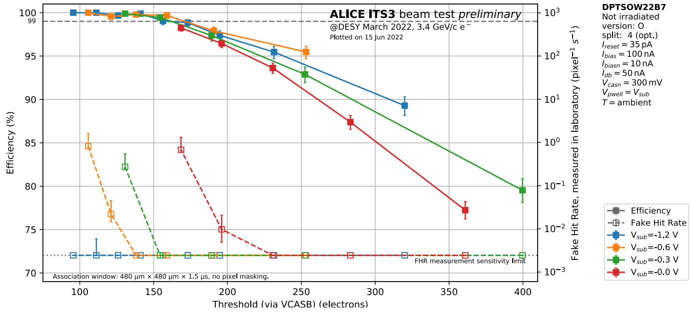
First submission in TJ 65 nm within CERN EP R&D WP1.2

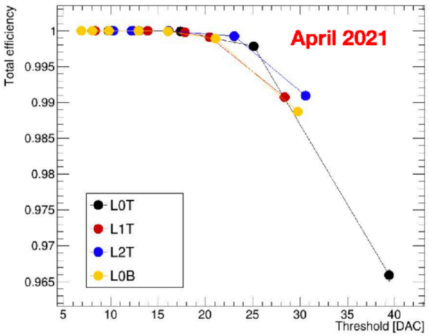


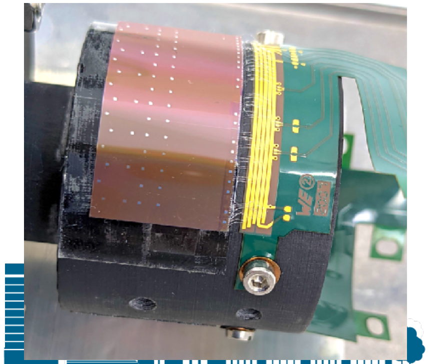
https://cds.cern.ch/record/2644611
https://arxiv.org/abs/2105.13000

https://indico.cern.ch/event/1071914/
https://indico.cern.ch/event/1156197/

Efficiency versus bending radii with bent ALPIDE (test beam data)







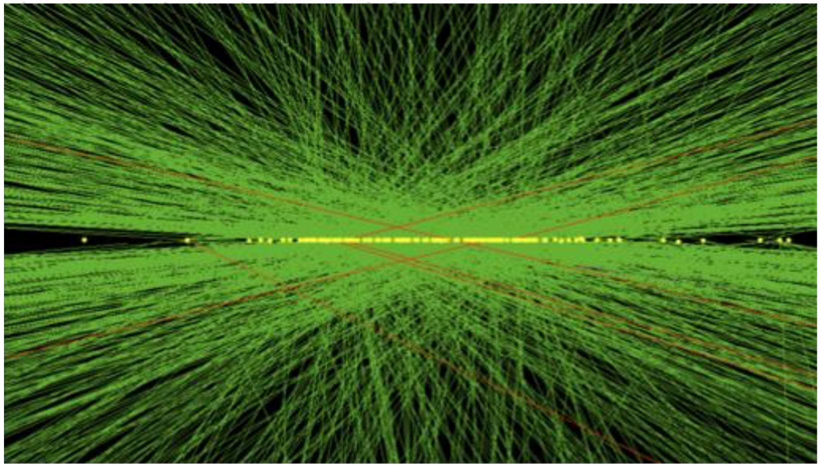
4D trackers

Why adding timing to 3D trackers?

- ☐ At the HL-LHC, 150-200 pile-up events per bunch crossing
  - Average distance between vertices = 500 µm
  - Timing RMS spread = 150 ps

- ☐ Typical vertex separation resolution along the beam pipe 250 – 300 µm

→ 10-15% of the vertices will be composed of overlapping events

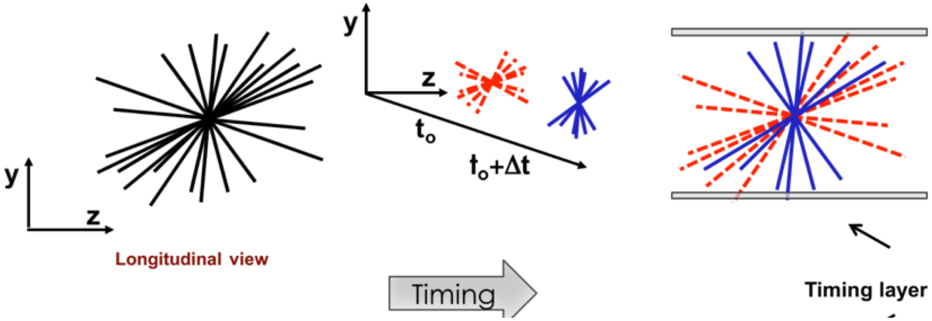


The effect of timing information

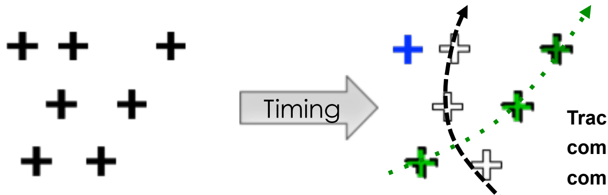
- Timing in the event reconstruction → Timing layers (state-of-the-art)
  - Timing associated to each crossing track
  - Easiest implementation, only one timing layer needed
  - Overlapping events can be separated by means of an extra dimension

- Timing in track reconstruction → 4D tracking (the future)
  - Timing associated to each point along the track
  - Massive simplification of patter recognition, faster algorithms in very dense environments but massive increase of power consumption
    - Electronics needs to accurately measure timing in each pixel

Timing layers

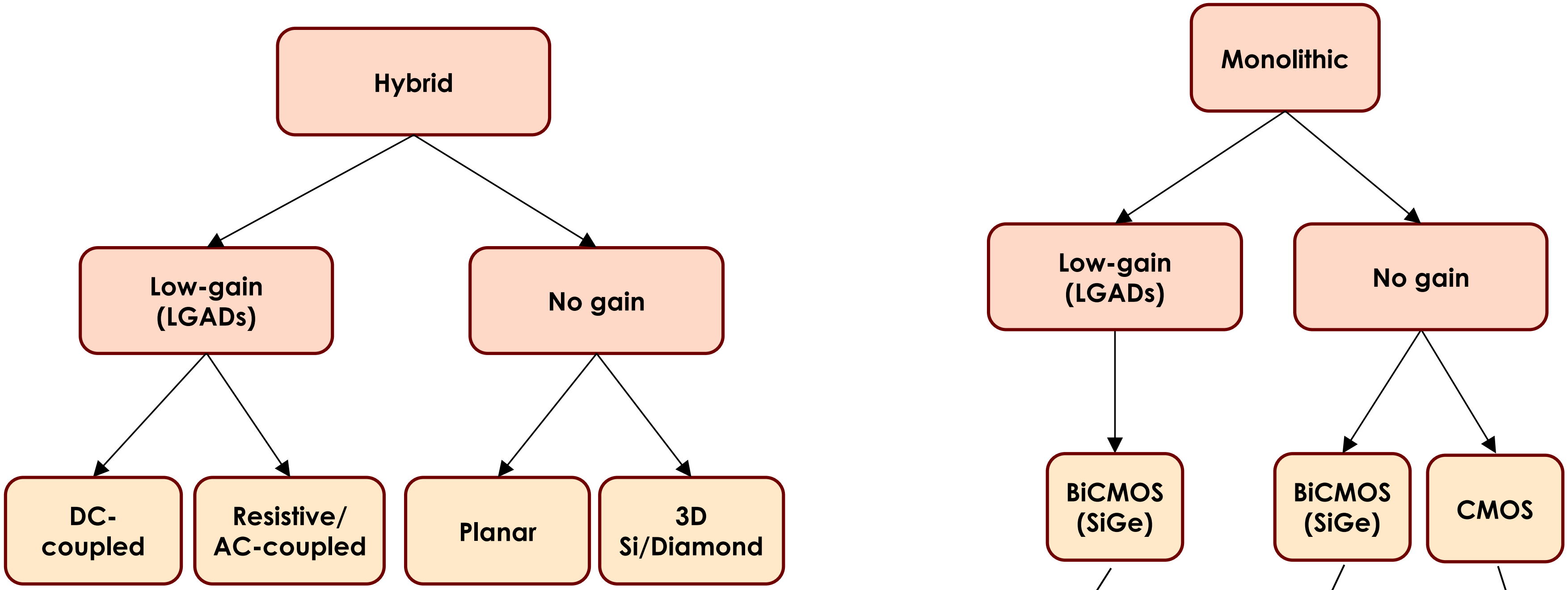


4D tracking

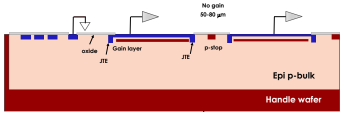


Tracks obtained combining only time-compatible points

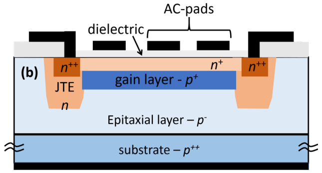
Ongoing R&D



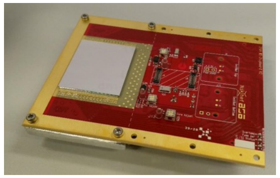
DC -coupled LGADs



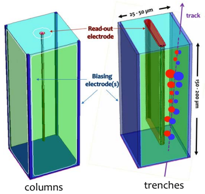
AC-coupled LGADs

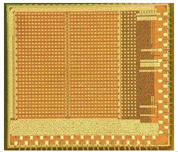


TimePix



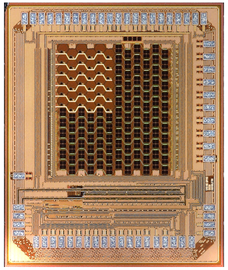
TimeSPOT



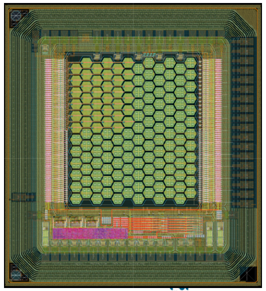


Monolith

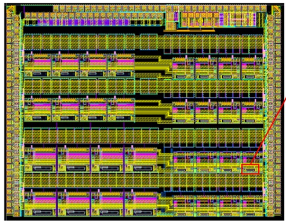
Image of first MONOLITH prototype:



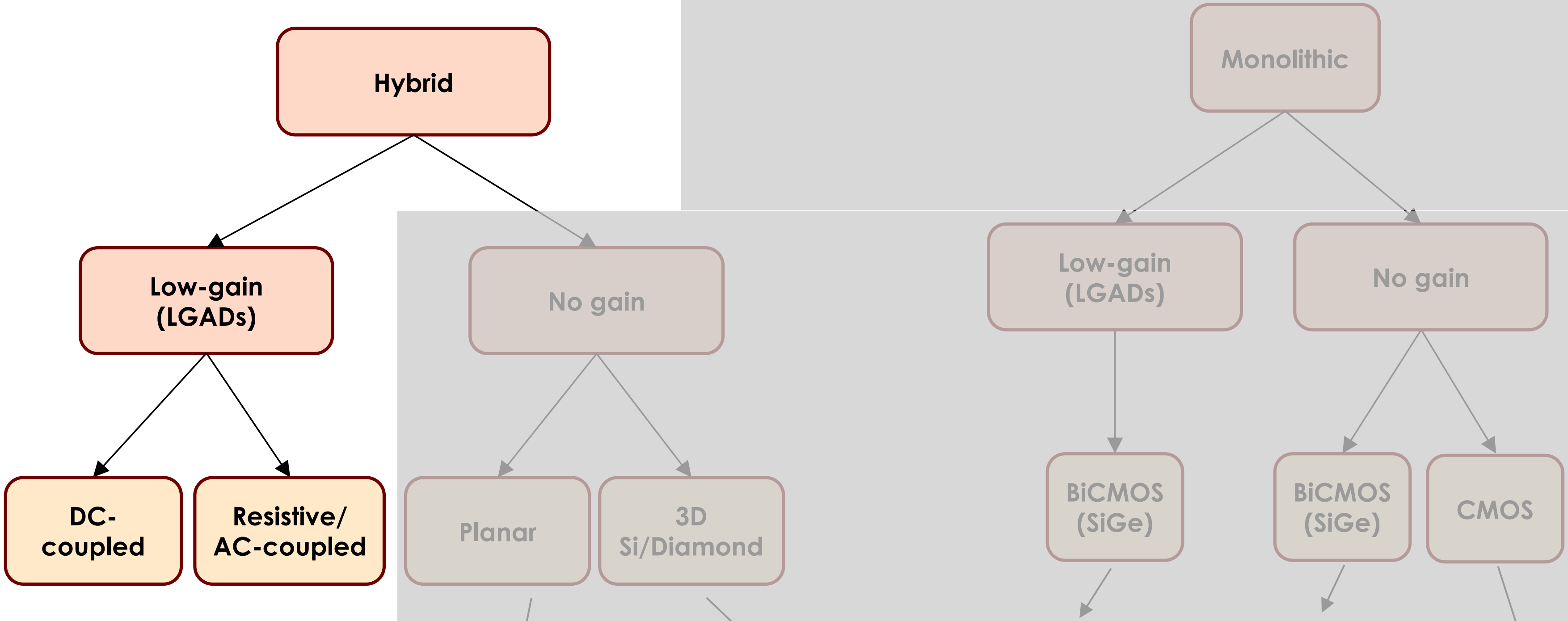
MonPicoAD



FASTPIX



Ongoing R&D



Hybrid

Low-gain (LGADs)

DC-coupled

Resistive/ AC-coupled

No gain

Planar

3D Si/Diamond

Monolithic

Low-gain (LGADs)

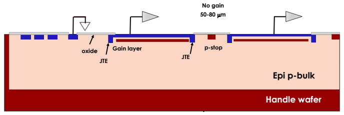
No gain

BiCMOS (SiGe)

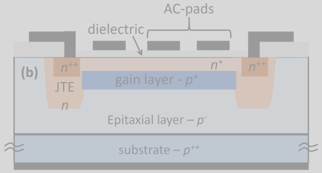
BiCMOS (SiGe)

CMOS

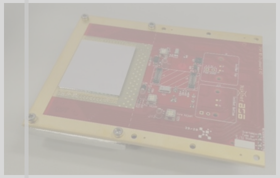
DC -coupled LGADs



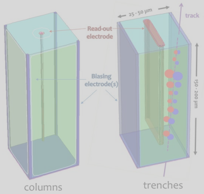
AC-coupled LGADs

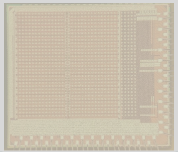


TimePix



TimeSPOT





Monolith

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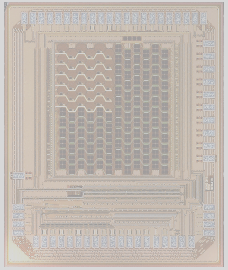
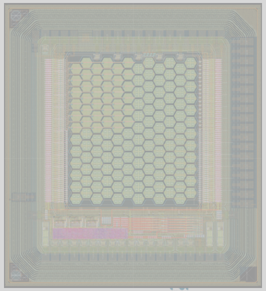


MonPicoAD



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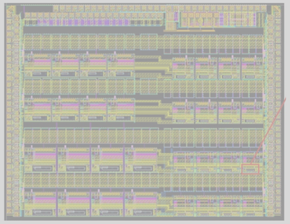
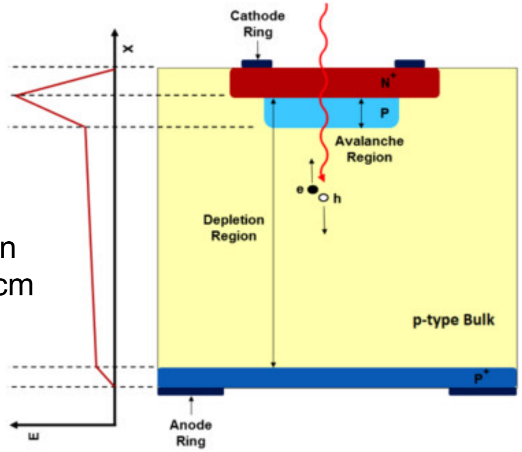


Low Gain Avalanche Detectors (LGAD) design

1. Take a planar n-in-p sensor → Parallel plate geometry, uniform v_d and E_w
2. Add a charge multiplication layer tuned to achieve low gain → Higher S/N
3. Make the sensor thin → uniform signal, fast rise time

→ LGAD sensors produce uniform signals with low jitter



Multiplication region
E = 300 kV/cm

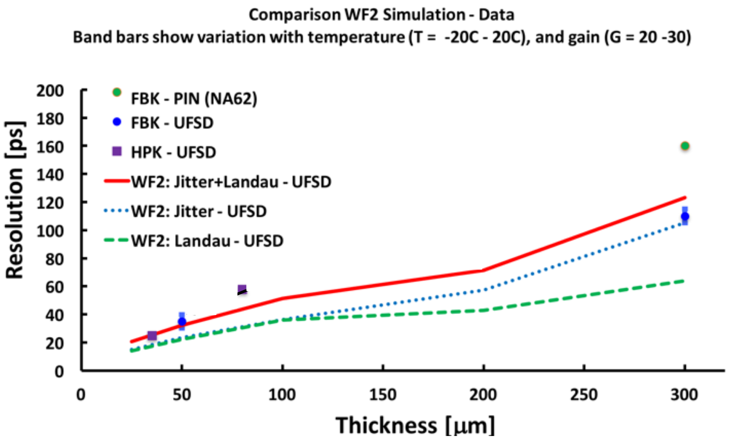
Drift region
E = 30 kV/cm

State-of-the-art LGAD for ATLAS and CMS
- Pitch: 1.3 x 1.3 mm^2
- Thickness: 50 µm
- Time resolution: ~25 ps (sensor)
- Radiation tolerance: ~ 2x10^{15} neutrons/cm^2

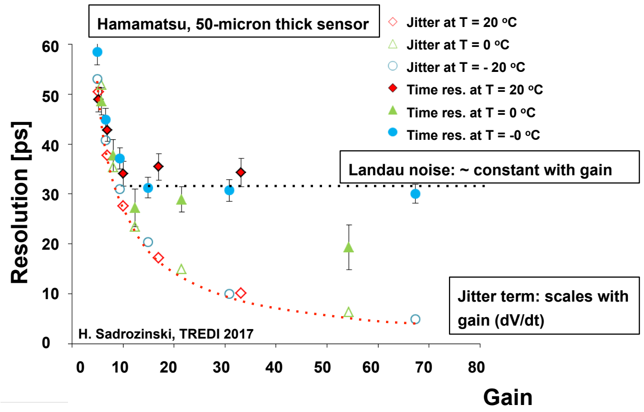
Established LGAD producers:
FBK, CNM, Hamamatsu
More recent additions/upcoming:
BNL, IHEP, Micron, Te2V

LGAD performance

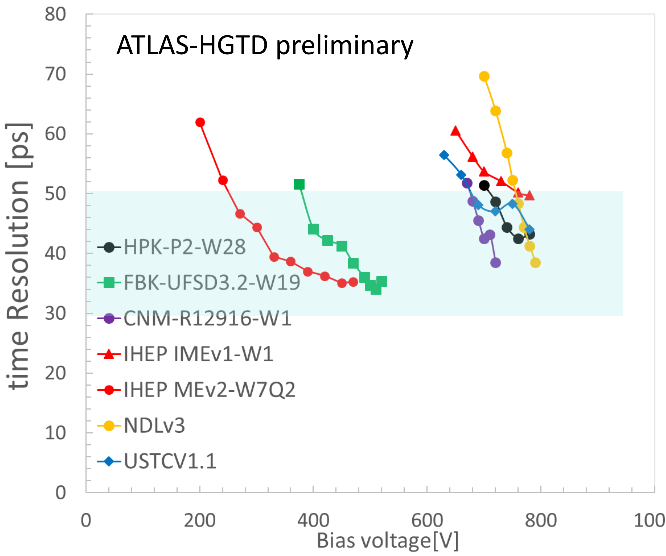
- ☐ Intrinsic temporal resolution (25-30 ps) reached for thickness ≲ 50 µm



UFSD from Hamamatsu: 30 ps time resolution,
Value of gain ~ 20



- ☐ Time resolution in the 30-50 ps range at 2.5x10^{15} MeV n$_{eq}$/cm^{2}
  - – C-enriched boron implants for gain layer to decrease acceptor removal



https://indico.cern.ch/event/587631/contributions/2471694/
https://indico.cern.ch/event/1088953/

ATLAS and CMS timing layers at the HL-LHC

- ☐ The ATLAS and CMS timing layers will be instrumented with LGAD sensors bump bonded to dedicated readout ASICs and associated infrastructure

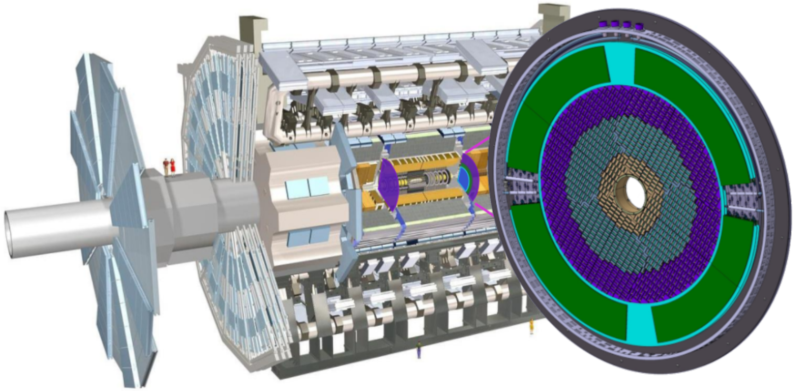
ATLAS

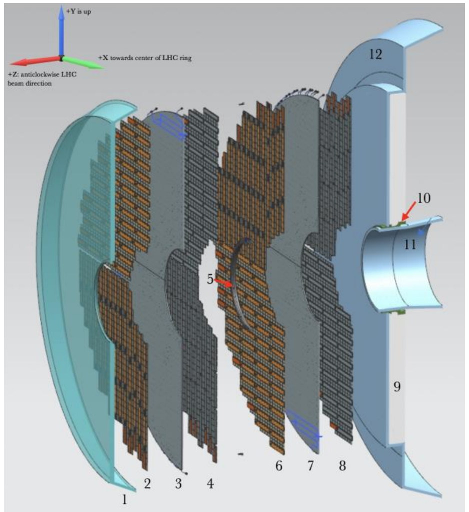
- ☐ 2 double-instrumented disks/end-cap
- ☐ Approx. 2.0 – 2.4 - 2.6 points/track
- ☐ 2.4 < |eta| < 4
- ☐ 120 mm < r < 640 mm , z = 350 cm
- ☐ 3.6M channels, 6.4 m^2

CMS

- ☐ 2 double-instrumented disks/end-cap
- ☐ Approx. 2 points/track
- ☐ 1.6 < |eta| < 3
- ☐ 315 mm < r < 1200 mm
- ☐ 8.5 M channels, 14 m^2

ALTIROC & ETIROC ASICs, 200-300 mW/cm^2
Resolution ~ 45 ps/hit



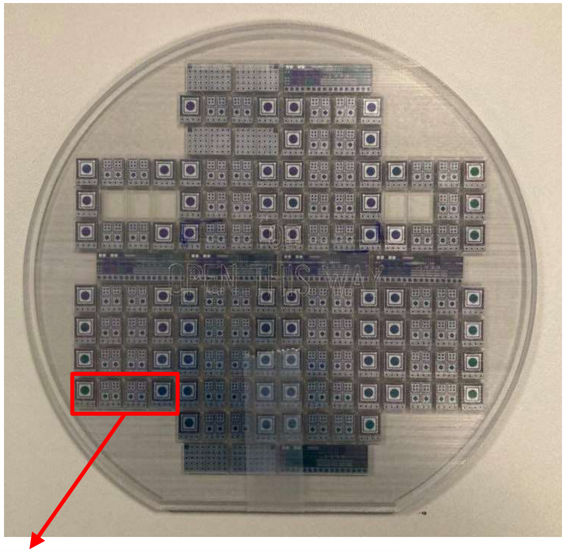


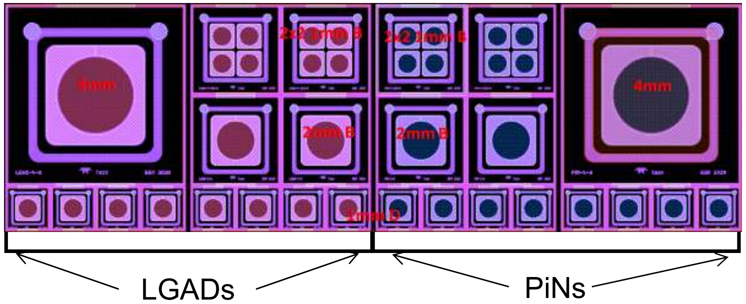
https://cds.cern.ch/record/2719855
https://cds.cern.ch/record/2667167/

UK development with Te2v

- Collaboration between the University of Birmingham, University of Oxford, RAL and the Open University working with the UK foundry at Teledyne e2v
  - Large production volume capability as a major producer of CCDs for space, astronomy and other scientific projects
- First batch of 22 wafers produced in 2021
  - 8 wafer flavours with different dose and energy of the gain implant
  - 4/2/1 mm size, 2x2 2 mm matrix, both LGAD and PIN
  - Characterisation well advanced, first results after irradiation

Wafer code	Normalised Dose (D)	Normalised Energy (E)
A	1.07	1.11
B	1.07	1.05
C	1.07	1.00
D	0.92	1.05
E	1.15	1.05
F	1.00	1.00
G	1.00	1.05
H	1.00	1.11

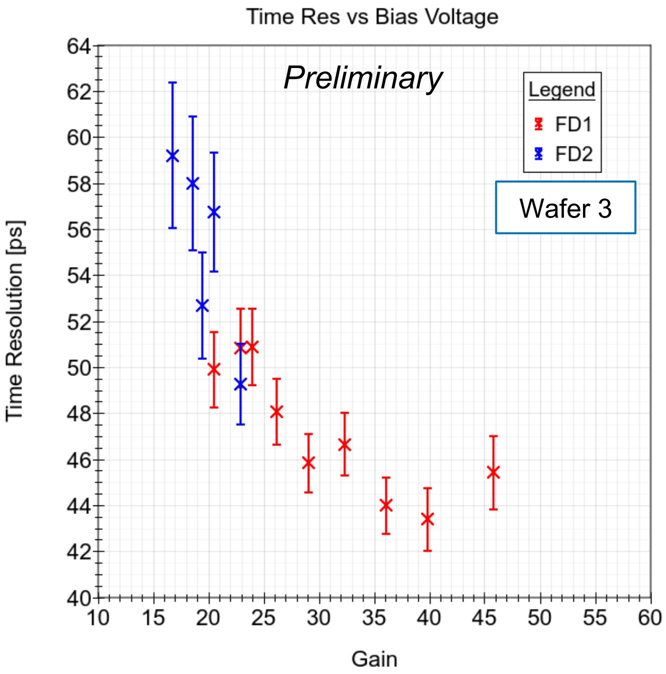




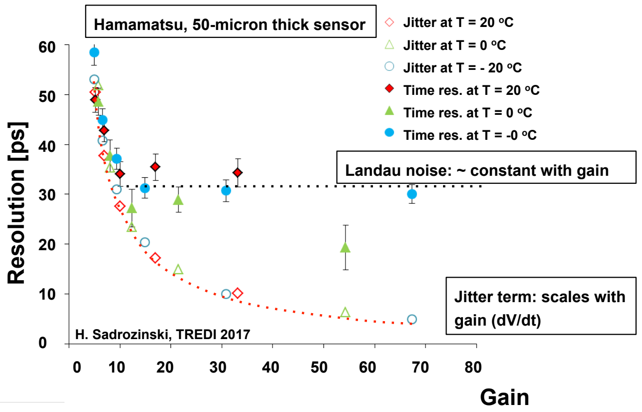
Gain & timing before before irradiation

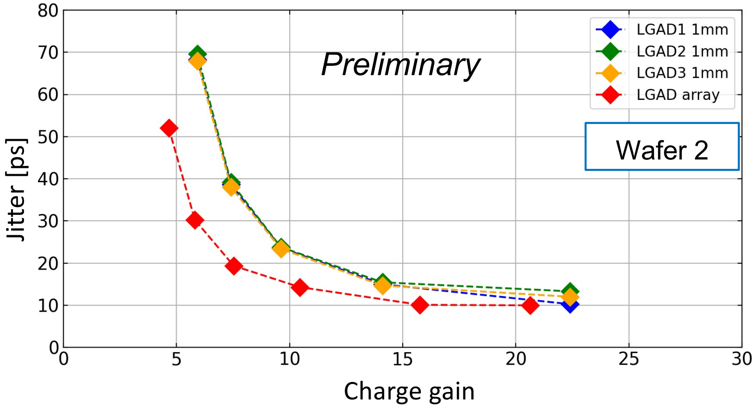
- ☐ Timing resolution calculated from coincidence signals from beta particles (Sr90)
- ☐ Gain measurement using TCT, comparing measured signal to a reference
- ☐ Jitter measurements performed using a transient current technique (TCT)

- ☐ Results before irradiation approach published values



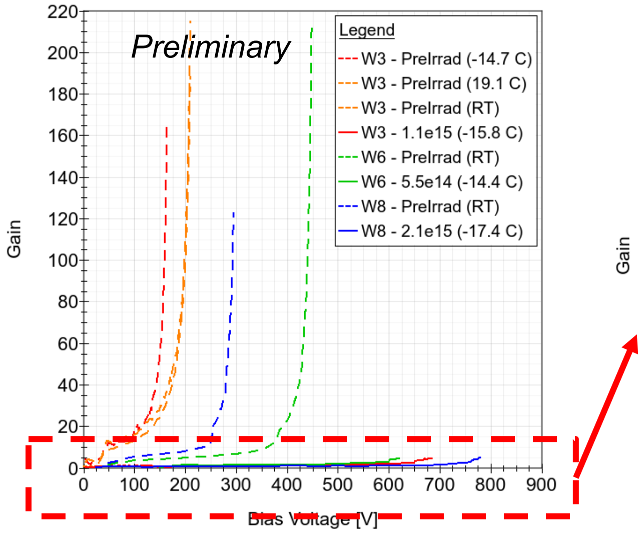
UFSD from Hamamatsu: 30 ps time resolution,
Value of gain ~ 20

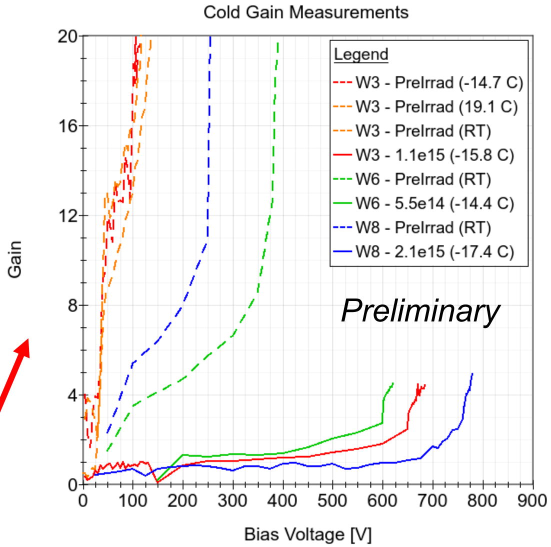


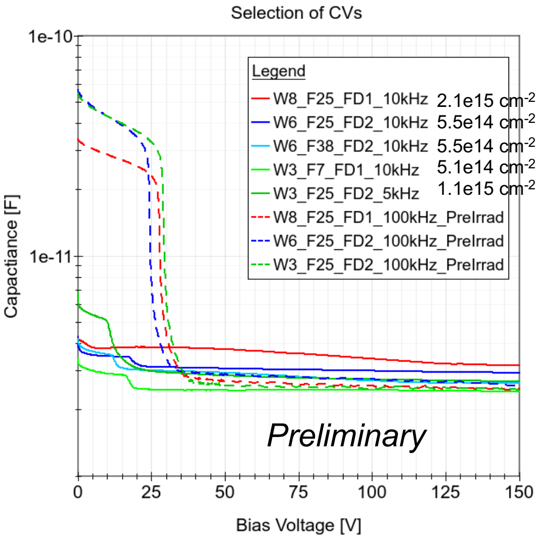


Results on proton irradiated devices

- Devices proton irradiated at MC40 cyclotron with 27 MeV protons in Birmingham (~0.5 to 2E15 n_{eq}/cm^2)
- After irradiation, gain is significantly lowered and is achieved at bias voltage of several hundred volts
- CV measurements indicate reduction of gain layer

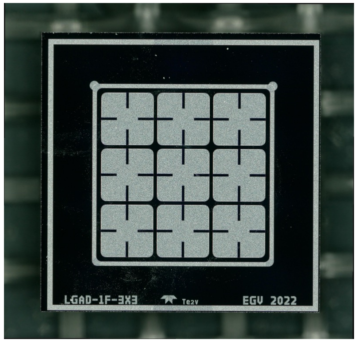




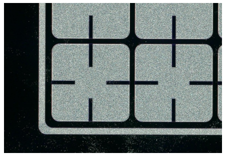


Second batch with Te2v

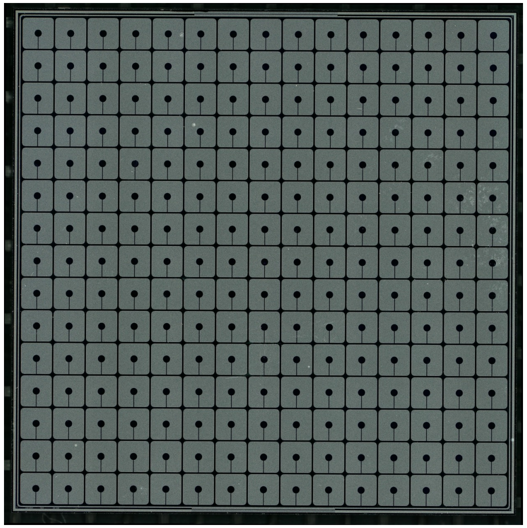
- Second batch of LGAD wafers produced by Teledyne e2v received in December for testing
- 4 different combinations of manufacturing parameters, guided by Batch 1 results
- Wider range of layouts and arrangements
    - Single device, 2x2 and 3x3 arrays, full size 15 x 15 array



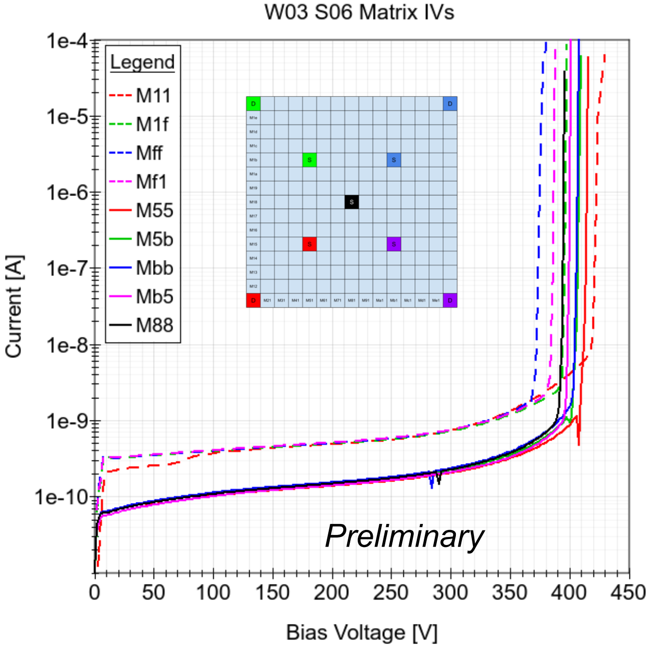
3x3 array for device cross-talk measurements



Adjusted surface metallisation for edge-effect measurements with TCT



full scale 15x15 array with 1.3x1.3 mm^2 devices



From timing layers to 4D trackers

- Achieving ~ few μm spatial resolution and ~ tens ps time resolution simultaneously, for large area systems that operate in high radiation environments, within a low to moderate power budget is a complex challenge.

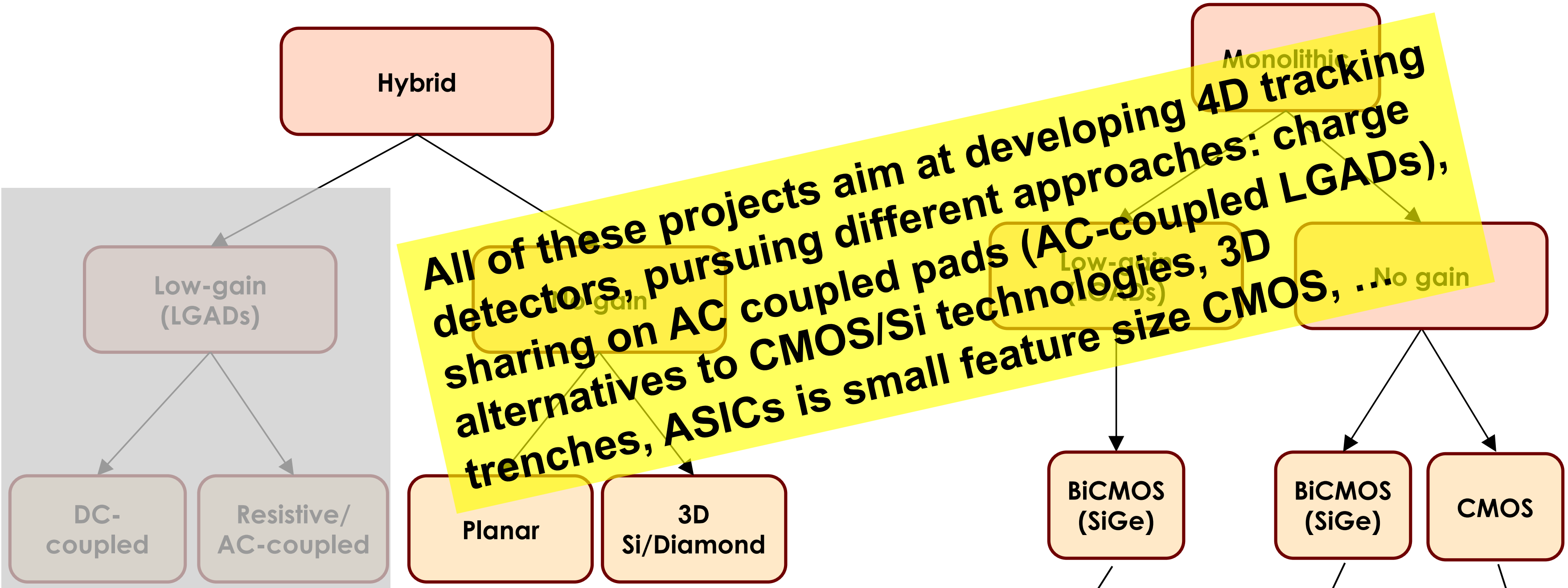
- Smaller CMOS technology nodes promise less power per channel and higher radiation hardness
  - But smaller pixels → more pixels → more power

- Time resolution demonstrated down to ~ 30 ps in small ASIC and sensor prototypes with pixel pitch < 100 μm within the target power budget

- But we want to build large area systems (tens to hundreds of square meters)
  - Timing challenge scales with area (starting at the chip level)

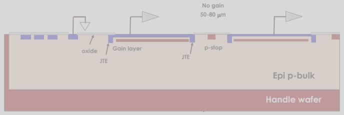
- System level development are crucial to achieve the target temporal resolution
  - Power and clock distribution, cooling, data transmission, …

Ongoing R&D

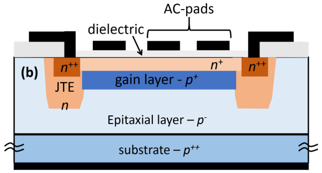


All of these projects aim at developing 4D tracking detectors, pursuing different approaches: charge sharing on AC coupled pads (AC-coupled LGADs), alternatives to CMOS/Si technologies, 3D trenches, ASICs is small feature size CMOS, …

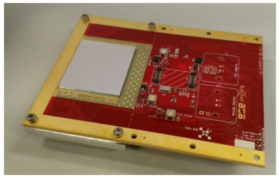
DC -coupled LGADs



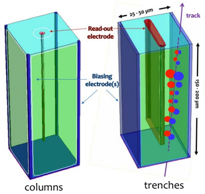
AC-coupled LGADs

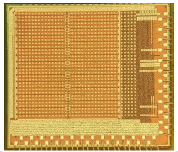


TimePix



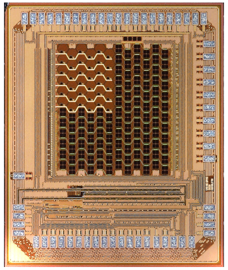
TimeSPOT



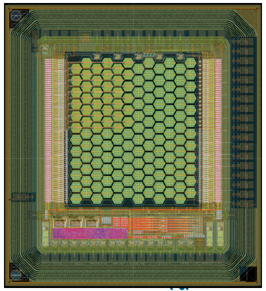


Monolith

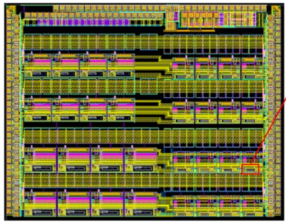
Image of first MONOLITH prototype:



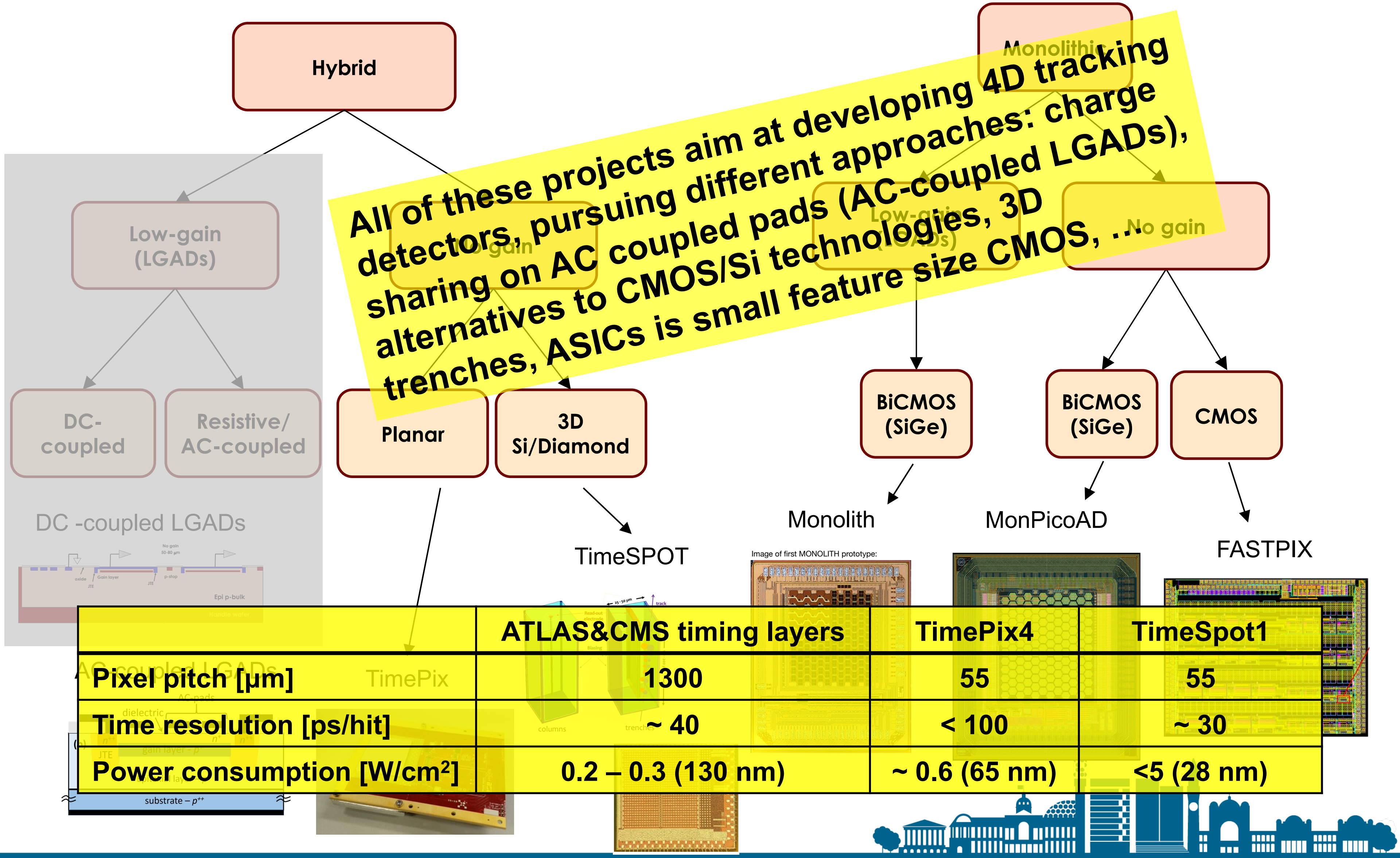
MonPicoAD



FASTPIX



Ongoing R&D



All of these projects aim at developing 4D tracking detectors, pursuing different approaches: charge sharing on AC coupled pads (AC-coupled LGADs), alternatives to CMOS/Si technologies, 3D trenches, ASICs is small feature size CMOS, …

	ATLAS&CMS timing layers	TimePix4	TimeSpot1
Pixel pitch [μm]	1300	55	55
Time resolution [ps/hit]	~ 40	< 100	~ 30
Power consumption [W/cm²]	0.2 – 0.3 (130 nm)	~ 0.6 (65 nm)	<5 (28 nm)

Conclusion

- Silicon detectors are the only technology that can satisfy the requirements of vertex and tracking detectors at collider experiments

- A large R&D programme is ongoing to further improve their performance to match the challenges of future applications

- Recent and new developments in CMOS sensors will provide the breakthrough technology for future vertex and tracking matching the requirements of most applications

- The addition of high time precision to the fine granularity of pixel detectors is the key innovation for tracking at high luminosity colliders

Backup

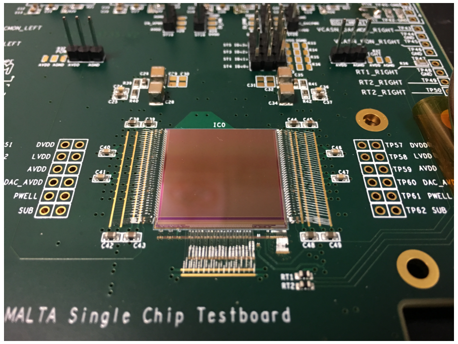
MALTA sensor development

MALTA sensor (2018)
180 nm TJ CMOS imaging technology
High resistivity epi-layer, 25 - 30 µm thick
36.4 µm pixel pitch
512 x 512 pixel matric, 20 x 22 mm^2
Novel asynchronous readout architecture for low power consumption and high hit rate

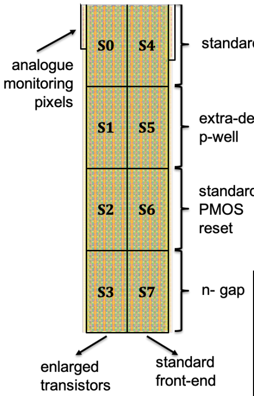
Mini-MALTA sensor (2019)
5 x 1.7 mm^2 demonstrator
64 x 16 MALTA pixels
Different modifications to sensor layout and FE electronics implemented in 8 sectors

MALTA Cz sensor (2019)
Full size demonstrator (20 x 22 mm^2) on epi and Czochralski substrate
Different sensor layout flavours
Addition of slow control interface

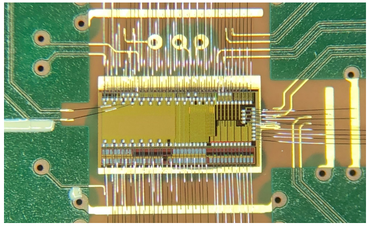
MALTA2 (2020)
20 x 10 mm^2 size demonstrator
224 x 512 MALTA pixels
Further FE improvements



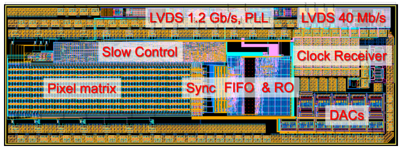
Pixel Matrix



Chip on MiniMALTA carrier board



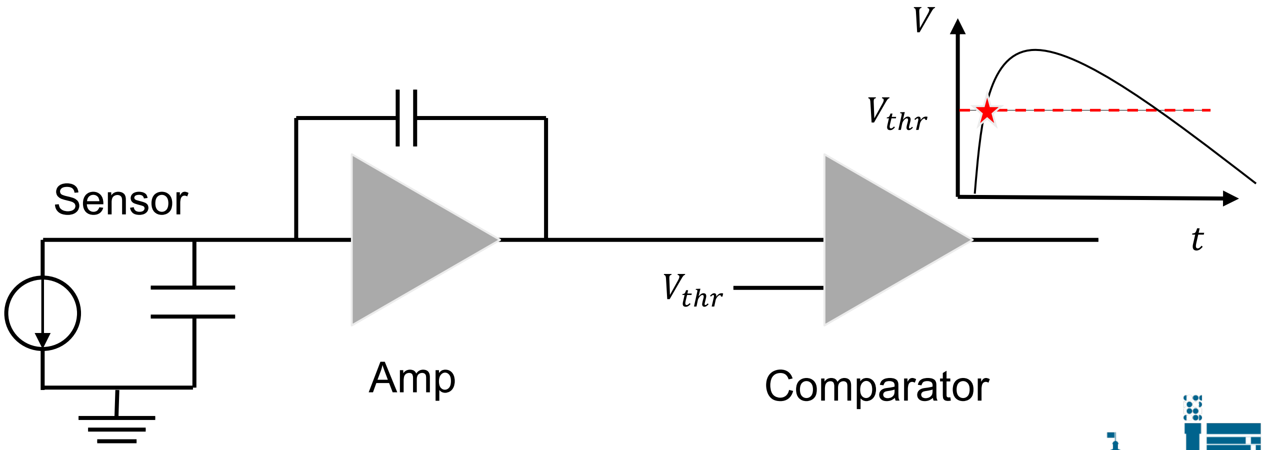
Chip Schematic



Time-tagging detectors

- The time resolution depends on multiple factors coming from the way the signal is generated in the sensor and then processed in the electronics
  - Time is set when the signal crosses the comparator threshold
  - A key element to good timing is uniformity of the signal

$$\sigma_t^2 = \underbrace{\sigma_{\mathrm{Land.\,TW}}^2 + \sigma_{\mathrm{Land.noise}}^2}_{\text{Physics}} + \underbrace{\sigma_{\mathrm{distorsion}}^2}_{\text{Sensor design}} + \underbrace{\sigma_{\mathrm{jitter}}^2 + \sigma_{\mathrm{TDC}}^2}_{\text{Electronics}}$$

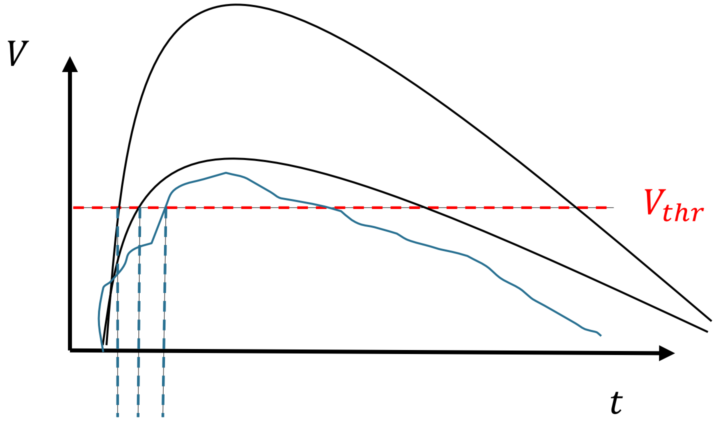


Time resolution

$$\sigma_t^2 = \sigma_{\mathrm{Land.\,TW}}^2 + \sigma_{\mathrm{Land.noise}}^2 + \sigma_{\mathrm{distorsion}}^2 + \sigma_{\mathrm{jitter}}^2 + \sigma_{\mathrm{TDC}}^2$$

- Terms depending on the physics governing the energy deposition
  - The charge distribution created by a MIP in the sensor varies event-by-event (Landau distribution)

- Overall change in signal magnitude → correctable time walk
  - Appropriate electronic circuit (ToT/ToA, CDF)
  - $\sigma_{\mathrm{Land.\,TW}}^2$ can be ignored



- Irregular current signal → non-correctable time walk
  - $\sigma_{\mathrm{Land.noise}}^2$ = physical limit to the time resolution

Time resolution

$$\sigma_t^2 = \xcancel{\sigma^2_{\text{Land. TW}}} + \sigma^2_{\text{Land.noise}} + \sigma^2_{\text{distorsion}} + \sigma^2_{\text{jitter}} + \sigma^2_{\text{TDC}}$$

- Term depending on sensor design

- Induced current signal on the electrode given by Ramo’s theorem

$$i(t) \propto q\, v_d\, E_w$$

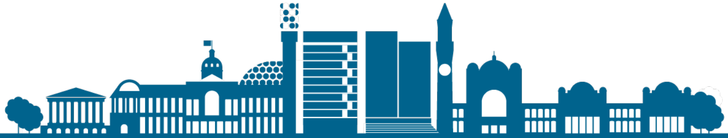
- The drift velocity, v_d , needs to be constant in the sensor volume, otherwise variation in signal shape depending in hit position → High E-filed = saturated drift velocity
- To have uniform weighting field, E_w, width ~ pitch >> thickness
- Parallel plate sensor geometry is required for uniform v_d and E_w

Time-tagging detectors

$$\sigma_t^2 = \xcancel{\sigma_{\mathrm{Land.\ TW}}^2} + \sigma_{\mathrm{Land.noise}}^2 + \sigma_{\mathrm{distorsion}}^2 + \sigma_{\mathrm{jitter}}^2 + \xcancel{\sigma_{\mathrm{TDC}}^2}$$

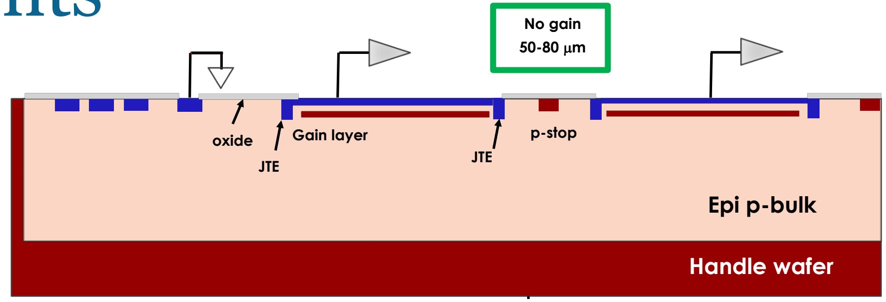
- Term depending on electronics
- σ_{TDC}^2 : term coming from TDC binning (analogue-to-digital conversion), typically small contribution, can be ignored
- $\sigma_{\mathrm{jitter}}^2$: mostly due to noise and the amplifier slew rate
  - Large, uniform signals
  - Low noise
  - Fast rise time

$$\sigma_{\mathrm{jitter}} \propto \frac{Noise}{dV/_{dT}} = \frac{t_{rise}}{S/_{N}}$$



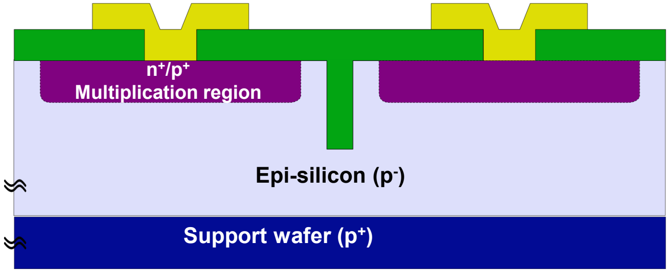
Further LGAD developments

- ☐ LGAD shortcomings
  - Large no-gain area between pads
  - Poor spatial resolution

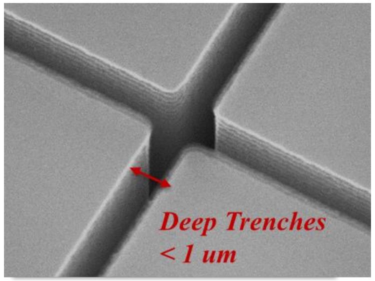


- ☐ Some small pitch developments:

Trench Isolated LGAD

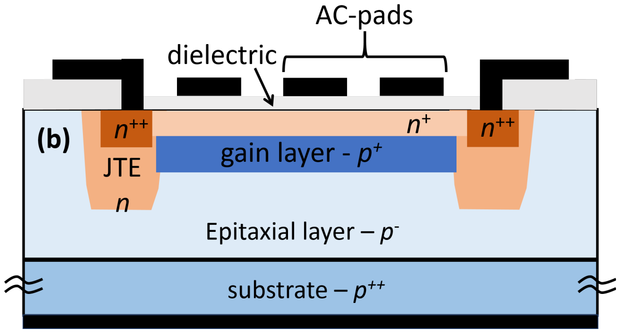


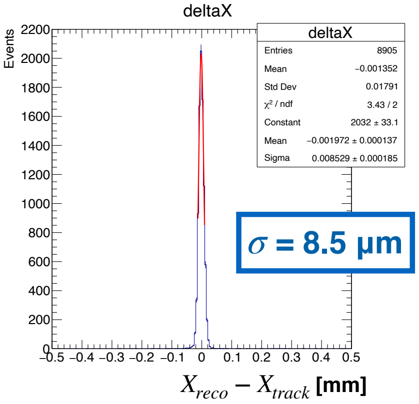
Prototype TI-LGAD with pitch down to 50 µm; no gain region <10 µm



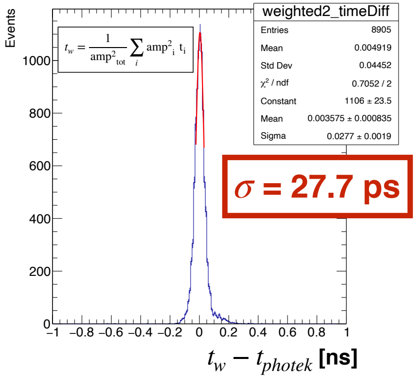
https://indico.cern.ch/event/1074989/contributions/4602011/

AC-LGAD





$\sigma = 8.5\ \mu m$



$$t_w = \frac{1}{\mathrm{amp}^2_{\mathrm{tot}}} \sum_i \mathrm{amp}^2_{\mathrm{i}}\ \mathrm{t_i}$$

$\sigma = 27.7\ \mathrm{ps}$

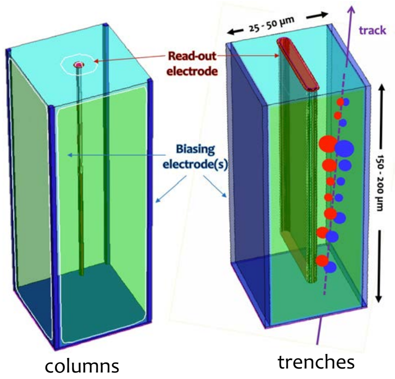
https://indico.cern.ch/event/1074989/contributions/4602013/

Fast-timing without gain layer

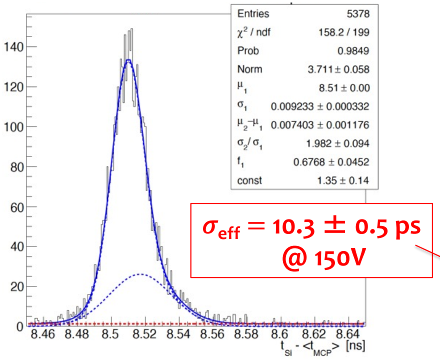
- The TimeSPOT project aims at developing a 4D detector concept using sensors without gain and fast ASIC is 28 nm CMOS tecchnology

- 3D trenched geometry
  - Time resolution of ~10-15 ps for 55 µm pitch pixels
  - Fully efficient at 20o angle
  - No performance degradation observed at 2E16 neq/cm2

- TimeSPOT1 ASIC
  - 32 x 32 pixel matrix (small area prototype) demonstrated timing performance around ~20 ps (AFE, TDC) with low-moderate power budget

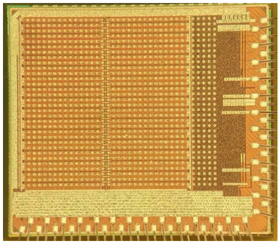


Irradiated @ 2.5 10^{16} n_{eq}/cm^2 , α_{tilt} = 0°



$\sigma_{eff} = 10.3 \pm 0.5$ ps @ 150V

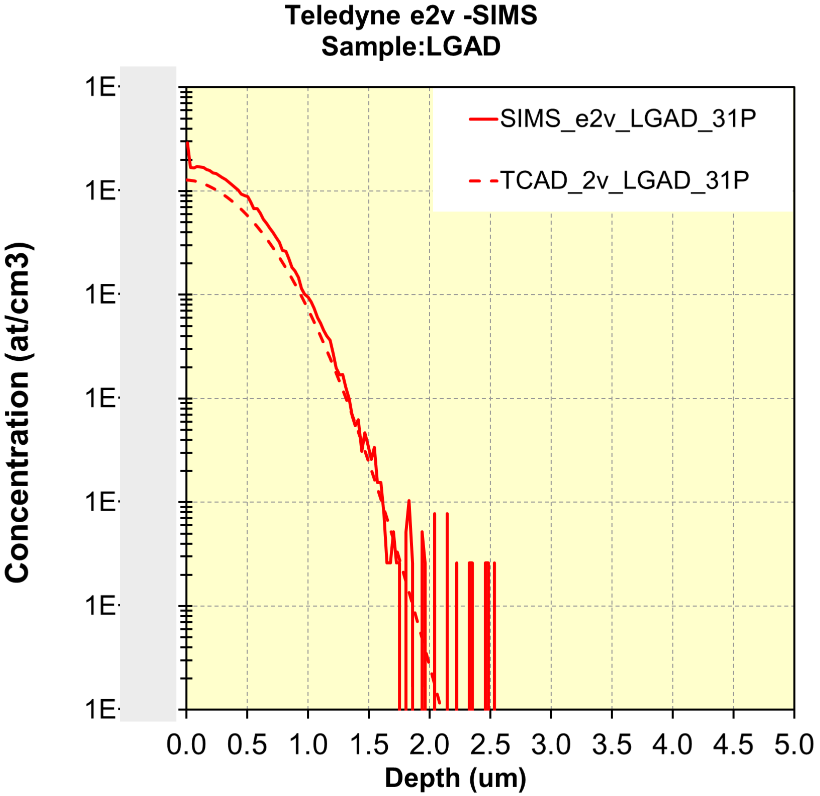
To be compared with 11 ps @ 100 V of the not-irradiated case

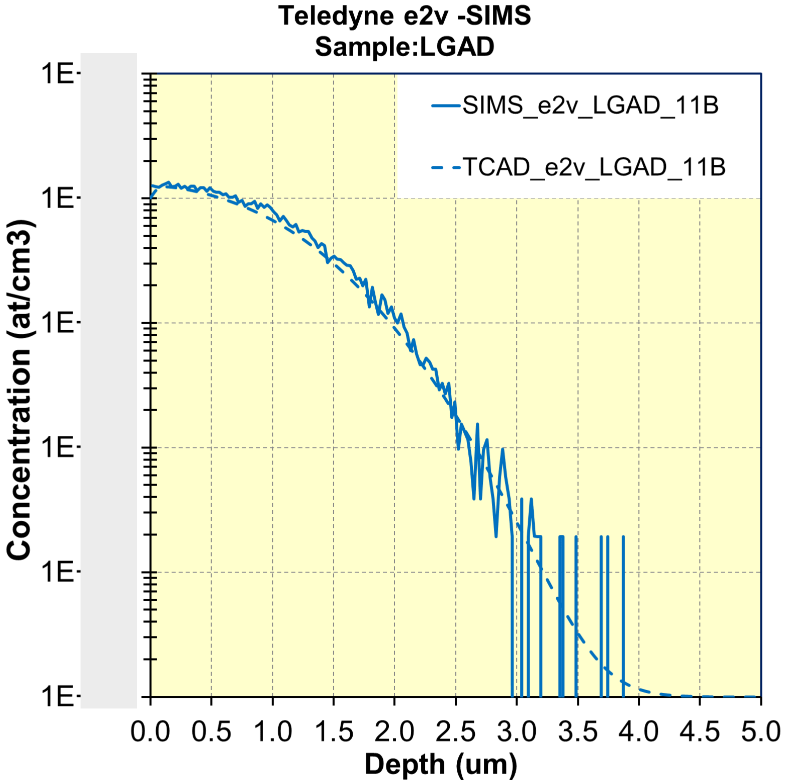


https://indico.cern.ch/event/1179742/
https://indico.cern.ch/event/1127562/contributions/4904519/

SIMS vs. TCAD

- SIMS performed on wafer 2 LGADs; results compared with TCAD simulations.
- Good agreement between measurements and developed SPROCESS description of Te2v fabrication process.

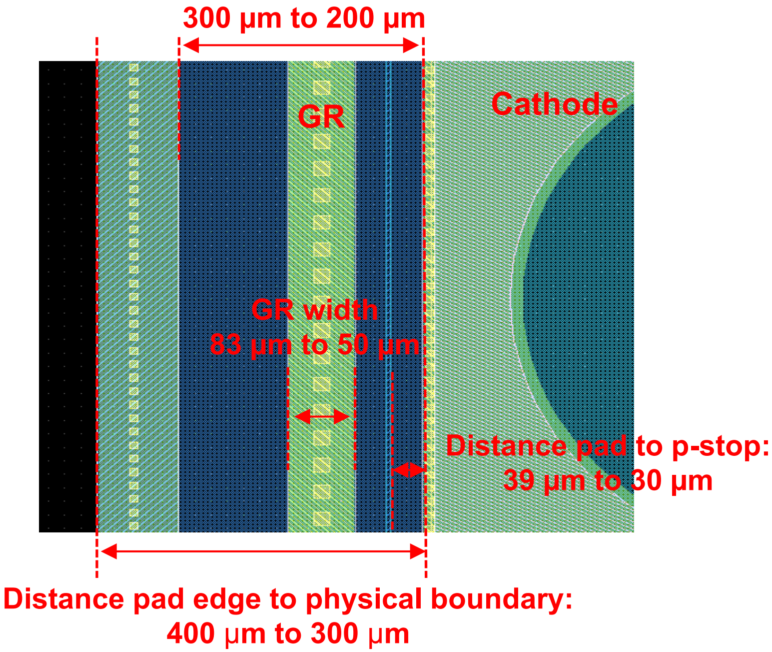


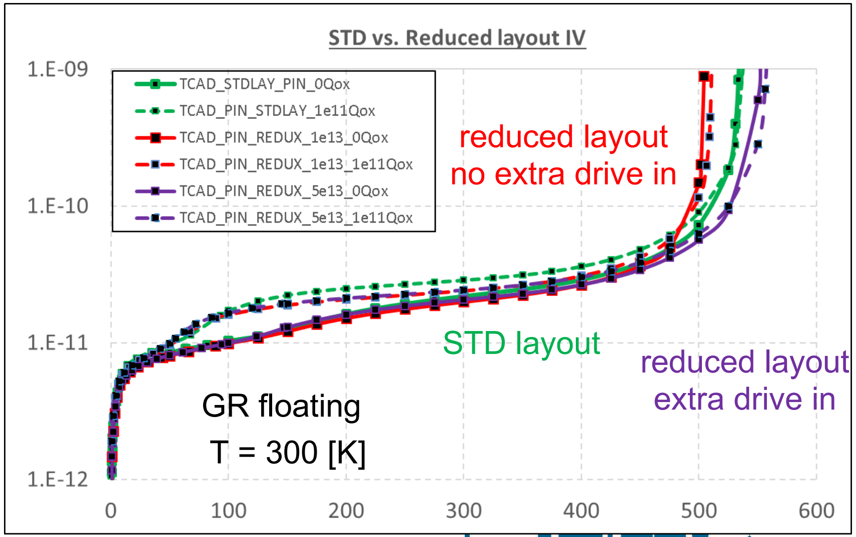


Plans for second submission

- Single cell modified to match requirements of ATLAS and CMS market survey.
  - Increased cell size to 1.3 mm x 1.3 mm.
  - Reduced max distance of pad edge to physical boundary to 300 µm.
  - Reduced distance of pad edge to PS to 30 µm.

- Reduced p-stop distance decreases the BV → TCAD simulations show that this can be compensated with increased JTE dose and drive in.





Plans for second submission

- Array of 15 x 15 cells built around modified basic cell.
- JTE edge to edge distance reduced from 114 µm to 96 µm.